

# Garda-3 Block Diagram

(Discrete)

CLK GEN.

IDT CV125PA  
(ICS 954206) 3

Mobile CPU

Yonah 478

G791/G792

19

Project code: 91.4P401.001

PCB P/N : 55.4P401.XXX

REVISION : 06208-2

(Hannstar, GCE)

DATE:2006/07/??

PCB STACKUP

TOP  
VCC  
S  
S  
GND  
BOTTOM

SYSTEM

TPS51120

40

INPUTS

OUTPUTS

DCBATOUT

5V\_S5  
3D3V\_S5

SYSTEM DC/DC

APL5912

43

INPUTS

OUTPUTS

1D8V\_S3

1D05V\_S0

TPS51116

41

DCBATOUT

1D8V\_S3  
DDR\_VREF\_S0

APL5332KAC

3D3V\_S0

2D5V\_S0

43

APL5912

1D8V\_S3

1D5V\_S0

43

MAXIM CHARGER

ISL6255

42

INPUTS

OUTPUTS

DCBATOUT

CHG\_PWR  
18V 4.0A

UP+5V

5V 100mA

CPU

ISL6262

38,39

INPUTS

OUTPUTS

DCBATOUT

VCC\_CORE\_S0  
0~1.3V  
44A

ATI M52 DC/DC

ISL6269

52

INPUTS

OUTPUTS

DCBATOUT

VGA\_CORE\_S0

APL5331

43

1D8V\_S0

1D2V\_S0

BOM

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLOCK DIAGRAM

Size

A3

Document Number

AG3

Rev

2

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A

B

ICH7M Integrated Pull-up  
and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0]	ICH7 internal 20K pull-ups
LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

3

ICH7M IDE Integrated Series  
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

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Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.

C

954305D 27Mhz/LCDCLK Spread  
and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+0.25 Center
1	0	0	1	+0.5 Center
1	0	1	0	+0.75 Center
1	0	1	1	+1.0 Center
1	1	0	0	+0.25 Center
1	1	0	1	+0.5 Center
1	1	1	0	+0.75 Center
1	1	1	1	+1.0 Center

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PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
1410	22	A->G	0
MiniPCI	21	A/C B/D -> E	1
LAN	23	A -> H	2
1394	17	A->B, B->F,	3

History

D

E

Calistoga Strapping Signals and  
Configuration

EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading  
edge of the Calistoga GMCH PWORK in signal.

BOM

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reference

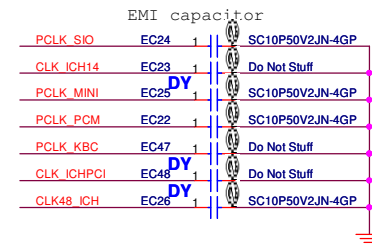
Size  
A3

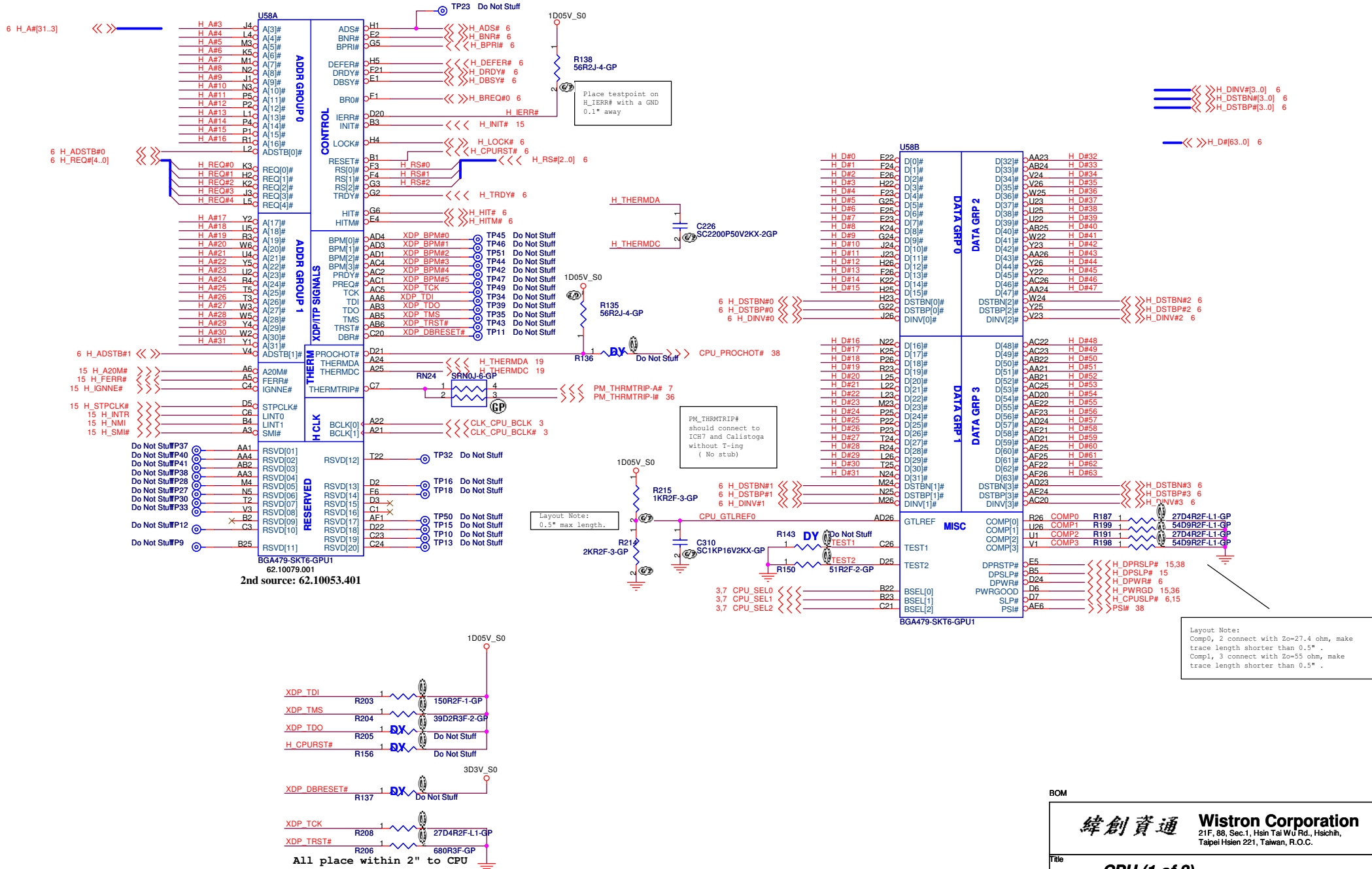
Document Number  
AG3

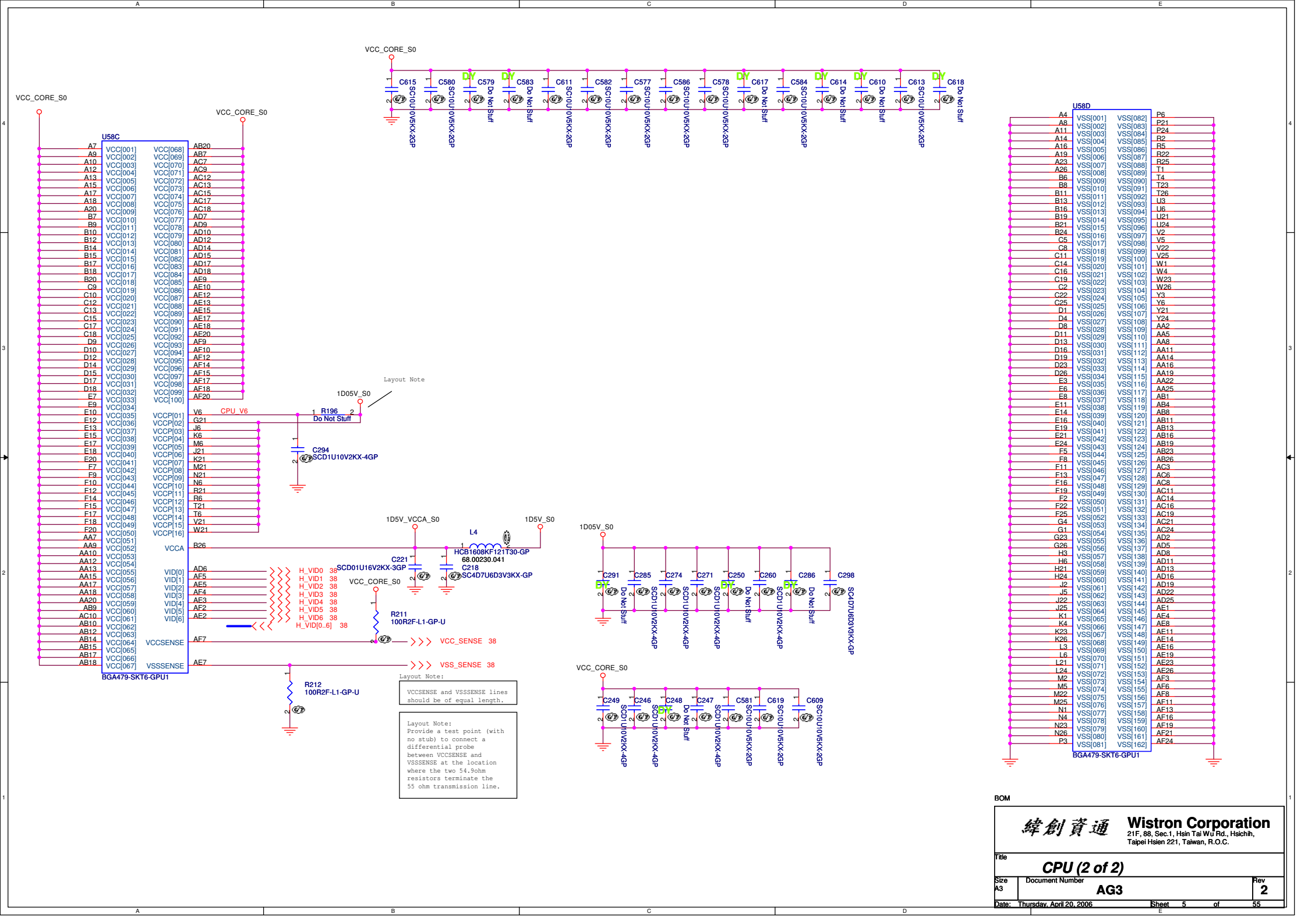
Rev  
2

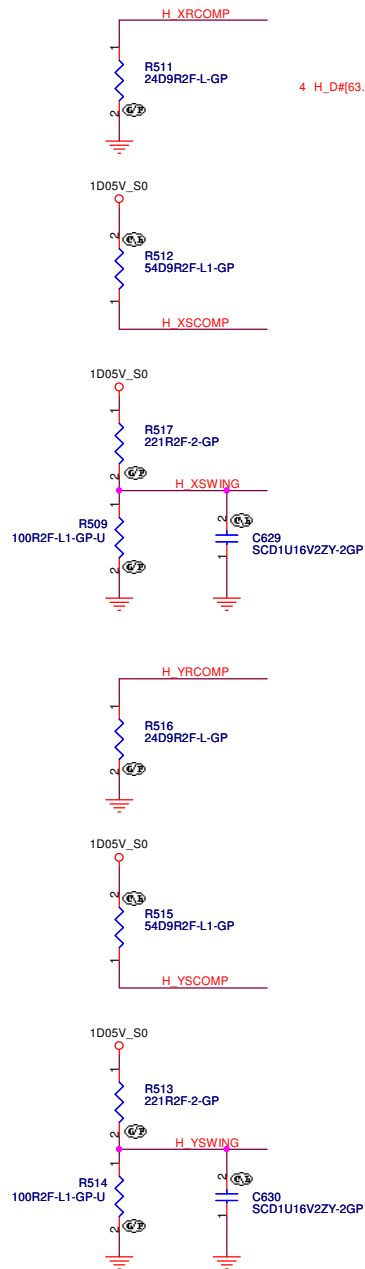
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Place them near to the chip ( < 0.5")

4 H\_D#[63..0] <<<>

3 CLK\_MCH\_BCLK# <<<>  
3 CLK\_MCH\_BCLK# <<<>

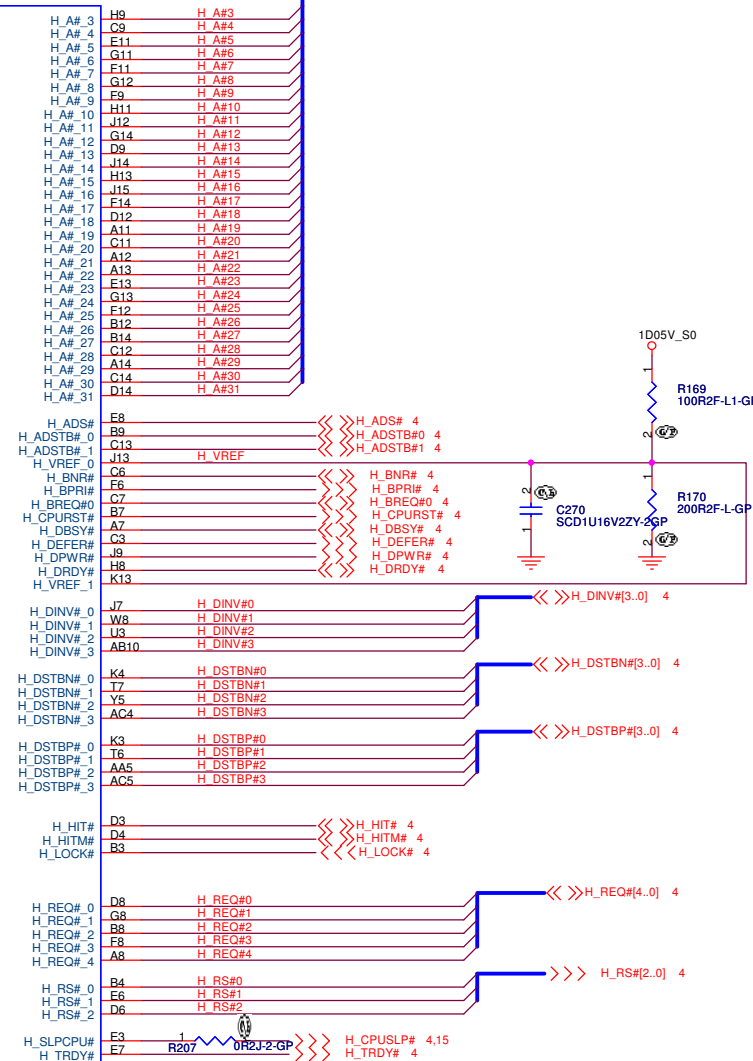
H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	K2	H_D#_4
H_D#5	G1	H_D#_5
H_D#6	G2	H_D#_6
H_D#7	K9	H_D#_7
H_D#8	K1	H_D#_8
H_D#9	K7	H_D#_9
H_D#10	J8	H_D#_10
H_D#11	H4	H_D#_11
H_D#12	J3	H_D#_12
H_D#13	K11	H_D#_13
H_D#14	G4	H_D#_14
H_D#15	T10	H_D#_15
H_D#16	T3	H_D#_16
H_D#17	U7	H_D#_17
H_D#18	U9	H_D#_18
H_D#19	U11	H_D#_19
H_D#20	T11	H_D#_20
H_D#21	T11	H_D#_21
H_D#22	W9	H_D#_22
H_D#23	T1	H_D#_23
H_D#24	T8	H_D#_24
H_D#25	T4	H_D#_25
H_D#26	W7	H_D#_26
H_D#27	U5	H_D#_27
H_D#28	T9	H_D#_28
H_D#29	W6	H_D#_29
H_D#30	T5	H_D#_30
H_D#31	AB7	H_D#_31
H_D#32	AA9	H_D#_32
H_D#33	W4	H_D#_33
H_D#34	W3	H_D#_34
H_D#35	Y3	H_D#_35
H_D#36	Y7	H_D#_36
H_D#37	W5	H_D#_37
H_D#38	Y10	H_D#_38
H_D#39	AB8	H_D#_39
H_D#40	W2	H_D#_40
H_D#41	AA4	H_D#_41
H_D#42	AA7	H_D#_42
H_D#43	AA2	H_D#_43
H_D#44	AA6	H_D#_44
H_D#45	AA10	H_D#_45
H_D#46	Y8	H_D#_46
H_D#47	AA1	H_D#_47
H_D#48	AB4	H_D#_48
H_D#49	AC9	H_D#_49
H_D#50	AB11	H_D#_50
H_D#51	AC11	H_D#_51
H_D#52	AB3	H_D#_52
H_D#53	AC2	H_D#_53
H_D#54	AD1	H_D#_54
H_D#55	AD9	H_D#_55
H_D#56	AC1	H_D#_56
H_D#57	AD7	H_D#_57
H_D#58	AC6	H_D#_58
H_D#59	AB5	H_D#_59
H_D#60	AD10	H_D#_60
H_D#61	AD4	H_D#_61
H_D#62	AC8	H_D#_62
H_D#63		H_D#_63

H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSCOMP	U1	H_YSCOMP
H_YSWING	W1	H_YSWING

H_CLKIN	AG2	H_CLKIN
H_CLKIN#	AG1	H_CLKIN#

U56A

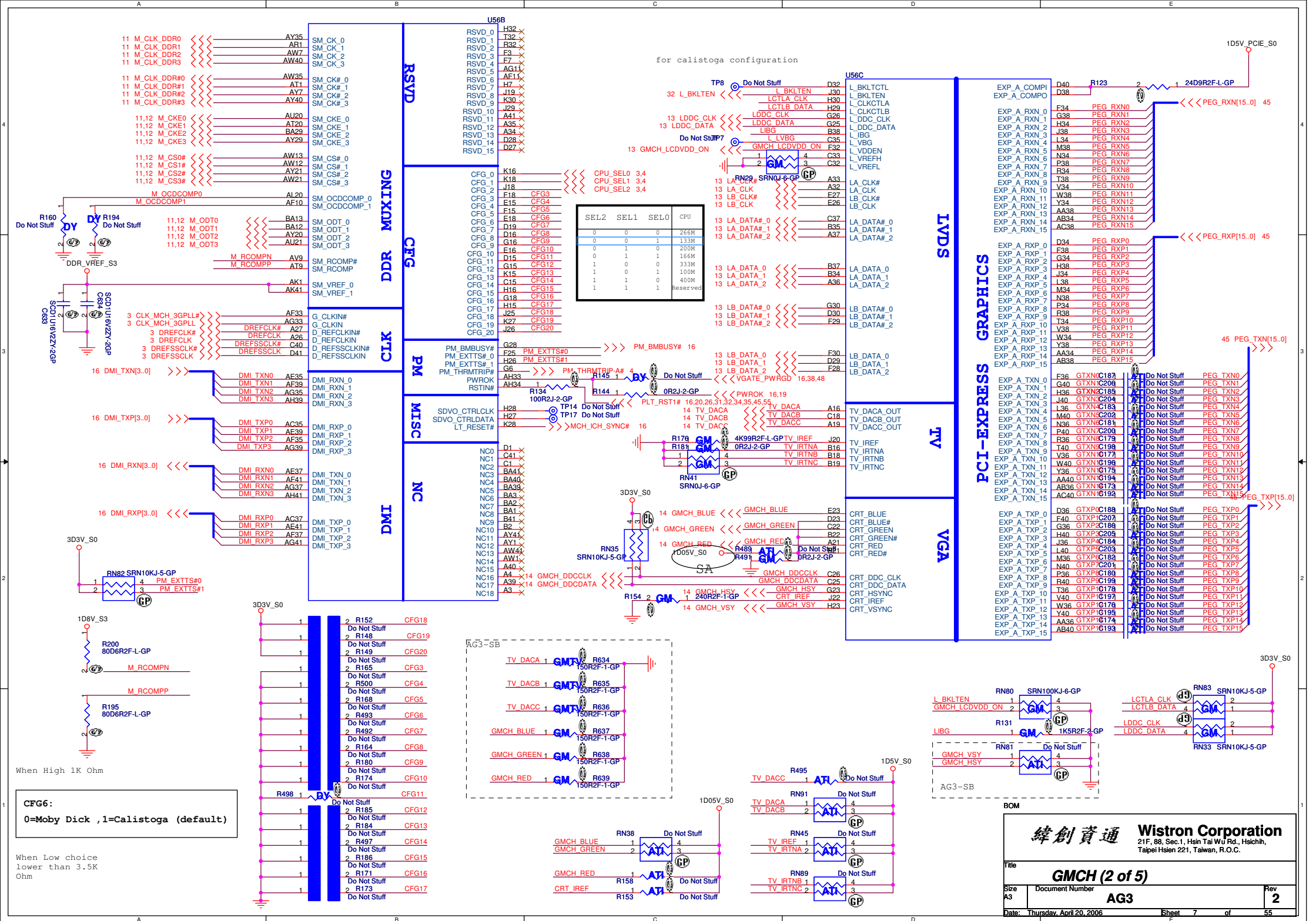
HOST



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<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title <b>GMCH (1 of 5)</b>	
Size A3	Document Number <b>AG3</b>
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11 M\_A\_DQ[63.0] <<<

M_A_DQ0	AJ35	SA_DQ0
M_A_DQ1	AJ34	SA_DQ1
M_A_DQ2	AM31	SA_DQ2
M_A_DQ3	AM33	SA_DQ3
M_A_DQ4	AJ38	SA_DQ4
M_A_DQ5	AK35	SA_DQ5
M_A_DQ6	AJ32	SA_DQ6
M_A_DQ7	AH31	SA_DQ7
M_A_DQ8	AN35	SA_DQ8
M_A_DQ9	AP33	SA_DQ9
M_A_DQ10	AF31	SA_DQ10
M_A_DQ11	AF31	SA_DQ11
M_A_DQ12	AN38	SA_DQ12
M_A_DQ13	AM36	SA_DQ13
M_A_DQ14	AM34	SA_DQ14
M_A_DQ15	AN33	SA_DQ15
M_A_DQ16	AK26	SA_DQ16
M_A_DQ17	AL27	SA_DQ17
M_A_DQ18	AM26	SA_DQ18
M_A_DQ19	AN24	SA_DQ19
M_A_DQ20	AK28	SA_DQ20
M_A_DQ21	AL28	SA_DQ21
M_A_DQ22	AM24	SA_DQ22
M_A_DQ23	AP26	SA_DQ23
M_A_DQ24	AF23	SA_DQ24
M_A_DQ25	AL22	SA_DQ25
M_A_DQ26	AP21	SA_DQ26
M_A_DQ27	AN20	SA_DQ27
M_A_DQ28	AL23	SA_DQ28
M_A_DQ29	AP24	SA_DQ29
M_A_DQ30	AF20	SA_DQ30
M_A_DQ31	AT21	SA_DQ31
M_A_DQ32	AR12	SA_DQ32
M_A_DQ33	AR14	SA_DQ33
M_A_DQ34	AP13	SA_DQ34
M_A_DQ35	AP12	SA_DQ35
M_A_DQ36	AT13	SA_DQ36
M_A_DQ37	AT12	SA_DQ37
M_A_DQ38	AL14	SA_DQ38
M_A_DQ39	AL12	SA_DQ39
M_A_DQ40	AK9	SA_DQ40
M_A_DQ41	AN7	SA_DQ41
M_A_DQ42	AK8	SA_DQ42
M_A_DQ43	AK7	SA_DQ43
M_A_DQ44	AP9	SA_DQ44
M_A_DQ45	AN9	SA_DQ45
M_A_DQ46	AT5	SA_DQ46
M_A_DQ47	AL5	SA_DQ47
M_A_DQ48	AY2	SA_DQ48
M_A_DQ49	AW2	SA_DQ49
M_A_DQ50	AP1	SA_DQ50
M_A_DQ51	AN2	SA_DQ51
M_A_DQ52	AY2	SA_DQ52
M_A_DQ53	AT3	SA_DQ53
M_A_DQ54	AN1	SA_DQ54
M_A_DQ55	AG7	SA_DQ55
M_A_DQ56	AG7	SA_DQ56
M_A_DQ57	AF3	SA_DQ57
M_A_DQ58	AG4	SA_DQ58
M_A_DQ59	AF6	SA_DQ59
M_A_DQ60	AG9	SA_DQ60
M_A_DQ61	AH6	SA_DQ61
M_A_DQ62	AF4	SA_DQ62
M_A_DQ63	AF3	SA_DQ63

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M_A_BS#0 11,12
SA_BS_1	AV14	M_A_BS#1 11,12
SA_BS_2	BA20	M_A_BS#2 11,12
SA_CAS#	AY13	M_A_CAS# 11,12
SA_DM_0	AJ33	M_A_DM0
SA_DM_1	AM35	M_A_DM1
SA_DM_2	AL26	M_A_DM2
SA_DM_3	AN22	M_A_DM3
SA_DM_4	AM14	M_A_DM4
SA_DM_5	AL9	M_A_DM5
SA_DM_6	AR3	M_A_DM6
SA_DM_7	AH4	M_A_DM7
SA_DQS_0	AK33	M_A_DQS0
SA_DQS_1	AT33	M_A_DQS1
SA_DQS_2	AN28	M_A_DQS2
SA_DQS_3	AM22	M_A_DQS3
SA_DQS_4	AN12	M_A_DQS4
SA_DQS_5	AN8	M_A_DQS5
SA_DQS_6	AP3	M_A_DQS6
SA_DQS_7	AG5	M_A_DQS7
SA_DQS#_0	AK32	M_A_DQS#0
SA_DQS#_1	AJ33	M_A_DQS#1
SA_DQS#_2	AN27	M_A_DQS#2
SA_DQS#_3	AM21	M_A_DQS#3
SA_DQS#_4	AM12	M_A_DQS#4
SA_DQS#_5	AL8	M_A_DQS#5
SA_DQS#_6	AN3	M_A_DQS#6
SA_DQS#_7	AH5	M_A_DQS#7
SA_MA_0	AY16	M_A_A0
SA_MA_1	AU14	M_A_A1
SA_MA_2	AW16	M_A_A2
SA_MA_3	BA16	M_A_A3
SA_MA_4	BA17	M_A_A4
SA_MA_5	AU16	M_A_A5
SA_MA_6	AV17	M_A_A6
SA_MA_7	AU17	M_A_A7
SA_MA_8	AW17	M_A_A8
SA_MA_9	AT16	M_A_A9
SA_MA_10	AU13	M_A_A10
SA_MA_11	AT17	M_A_A11
SA_MA_12	AV20	M_A_A12
SA_MA_13	AV12	M_A_A13
SA_RAS#	AW14	M_A_RAS# 11,12
SA_RCVENIN#	AK23	SA_RCVENIN#
SA_RCVENOUT#	AK24	SA_RCVENOUT#
SA_WE#	AY14	M_A_WE# 11,12

Place Test PAD Near to Chip as could as possible

11 M\_B\_DQ[63.0] <<<

M_B_DQ0	AK39	SB_DQ0
M_B_DQ1	AJ37	SB_DQ1
M_B_DQ2	AP39	SB_DQ2
M_B_DQ3	AR41	SB_DQ3
M_B_DQ4	AJ38	SB_DQ4
M_B_DQ5	AK38	SB_DQ5
M_B_DQ6	AN41	SB_DQ6
M_B_DQ7	AP41	SB_DQ7
M_B_DQ8	AT40	SB_DQ8
M_B_DQ9	AV41	SB_DQ9
M_B_DQ10	AJ38	SB_DQ10
M_B_DQ11	AJ38	SB_DQ11
M_B_DQ12	AP38	SB_DQ12
M_B_DQ13	AR40	SB_DQ13
M_B_DQ14	AW38	SB_DQ14
M_B_DQ15	AY38	SB_DQ15
M_B_DQ16	BA38	SB_DQ16
M_B_DQ17	AV36	SB_DQ17
M_B_DQ18	AR36	SB_DQ18
M_B_DQ19	AP36	SB_DQ19
M_B_DQ20	BA36	SB_DQ20
M_B_DQ21	AJ36	SB_DQ21
M_B_DQ22	AP35	SB_DQ22
M_B_DQ23	AP34	SB_DQ23
M_B_DQ24	AY33	SB_DQ24
M_B_DQ25	BA33	SB_DQ25
M_B_DQ26	AT31	SB_DQ26
M_B_DQ27	AJ29	SB_DQ27
M_B_DQ28	AJ31	SB_DQ28
M_B_DQ29	AW31	SB_DQ29
M_B_DQ30	AV29	SB_DQ30
M_B_DQ31	AW29	SB_DQ31
M_B_DQ32	AM19	SB_DQ32
M_B_DQ33	AL19	SB_DQ33
M_B_DQ34	AP14	SB_DQ34
M_B_DQ35	AN14	SB_DQ35
M_B_DQ36	AM17	SB_DQ36
M_B_DQ37	AM16	SB_DQ37
M_B_DQ38	AP15	SB_DQ38
M_B_DQ39	AL15	SB_DQ39
M_B_DQ40	AJ11	SB_DQ40
M_B_DQ41	AH10	SB_DQ41
M_B_DQ42	AJ9	SB_DQ42
M_B_DQ43	AN10	SB_DQ43
M_B_DQ44	AK13	SB_DQ44
M_B_DQ45	AH11	SB_DQ45
M_B_DQ46	AK10	SB_DQ46
M_B_DQ47	AJ8	SB_DQ47
M_B_DQ48	BA10	SB_DQ48
M_B_DQ49	AW10	SB_DQ49
M_B_DQ50	BA4	SB_DQ50
M_B_DQ51	AW4	SB_DQ51
M_B_DQ52	AY10	SB_DQ52
M_B_DQ53	AY9	SB_DQ53
M_B_DQ54	AW5	SB_DQ54
M_B_DQ55	AY5	SB_DQ55
M_B_DQ56	AV4	SB_DQ56
M_B_DQ57	AR5	SB_DQ57
M_B_DQ58	AK4	SB_DQ58
M_B_DQ59	AK3	SB_DQ59
M_B_DQ60	AT4	SB_DQ60
M_B_DQ61	AK5	SB_DQ61
M_B_DQ62	AJ5	SB_DQ62
M_B_DQ63	AJ3	SB_DQ63

DDR SYSTEM MEMORY B

SB_BS_0	AT24	M_B_BS#0 11,12
SB_BS_1	AV23	M_B_BS#1 11,12
SB_BS_2	AY28	M_B_BS#2 11,12
SB_CAS#	AR24	M_B_CAS# 11,12
SB_DM_0	AK36	M_B_DM0
SB_DM_1	AF38	M_B_DM1
SB_DM_2	AT36	M_B_DM2
SB_DM_3	BA31	M_B_DM3
SB_DM_4	AL17	M_B_DM4
SB_DM_5	AH8	M_B_DM5
SB_DM_6	BA5	M_B_DM6
SB_DM_7	AN4	M_B_DM7
SB_DQS_0	AM39	M_B_DQS0
SB_DQS_1	AT39	M_B_DQS1
SB_DQS_2	AJ35	M_B_DQS2
SB_DQS_3	AR29	M_B_DQS3
SB_DQS_4	AR16	M_B_DQS4
SB_DQS_5	AR10	M_B_DQS5
SB_DQS_6	AR7	M_B_DQS6
SB_DQS_7	AN5	M_B_DQS7
SB_DQS#_0	AM40	M_B_DQS#0
SB_DQS#_1	AJ39	M_B_DQS#1
SB_DQS#_2	AT35	M_B_DQS#2
SB_DQS#_3	AP29	M_B_DQS#3
SB_DQS#_4	AP16	M_B_DQS#4
SB_DQS#_5	AT10	M_B_DQS#5
SB_DQS#_6	AT7	M_B_DQS#6
SB_DQS#_7	AP5	M_B_DQS#7
SB_MA_0	AY23	M_B_A0
SB_MA_1	AW24	M_B_A1
SB_MA_2	AY24	M_B_A2
SB_MA_3	AR28	M_B_A3
SB_MA_4	AT27	M_B_A4
SB_MA_5	AT28	M_B_A5
SB_MA_6	AJ27	M_B_A6
SB_MA_7	AV28	M_B_A7
SB_MA_8	AV27	M_B_A8
SB_MA_9	AW27	M_B_A9
SB_MA_10	AV24	M_B_A10
SB_MA_11	BA27	M_B_A11
SB_MA_12	AY27	M_B_A12
SB_MA_13	AR23	M_B_A13
SB_RAS#	AJ23	M_B_RAS# 11,12
SB_RCVENIN#	AK16	SB_RCVENIN#
SB_RCVENOUT#	AK18	SB_RCVENOUT#
SB_WE#	AR27	M_B_WE# 11,12

Place Test PAD Near to Chip as could as possible

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

GMCH (3 of 5)

Size

A3

Document Number

AG3

Rev

2

Date

Thursday, April 20, 2006

Sheet

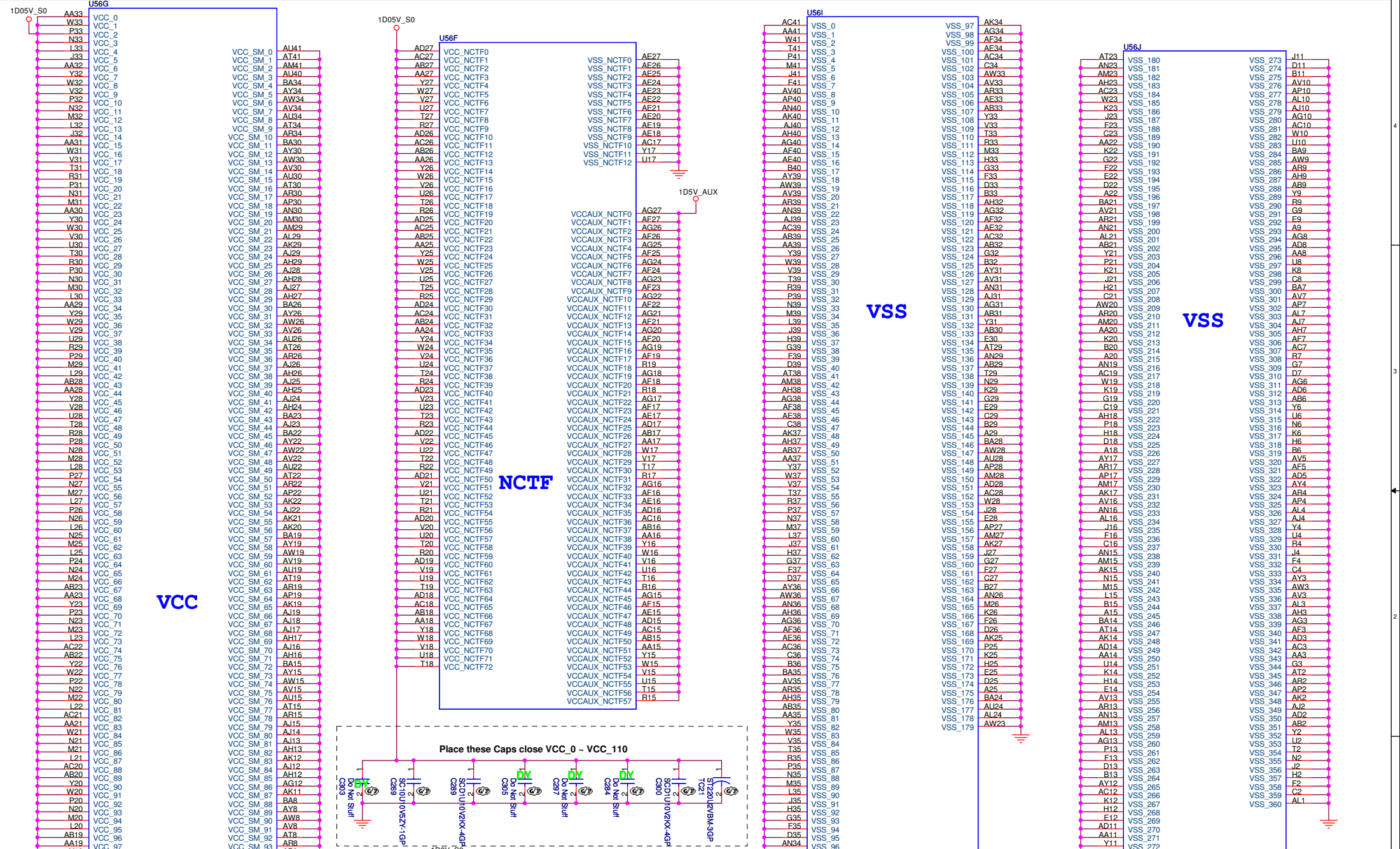
8

of

55









Put decap near power(0.9V) and pull-up resistor

DDR\_VREF\_S0

RN28

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_CKE2 7,11

M\_B\_BS#2 8,11

M\_A\_A13 8,11

M\_B\_A12

M\_B\_A9

R151

R157

R133

R142

56R2J-4-GP

M\_A\_A9

M\_B\_A8

M\_ODT1 7,11

M\_ODT3 7,11

RN31

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_B\_A5

M\_B\_A3

M\_B\_A1

M\_B\_A10

RN88

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_B\_RAS# 8,11

M\_CS2# 7,11

M\_ODT2 7,11

M\_B\_A13

RN87

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_B\_A4

M\_B\_A2

M\_B\_A0

M\_B\_BS#1 8,11

RN85

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_CKE3 7,11

M\_B\_A11

M\_B\_A7

M\_B\_A6

RN36

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_B\_BS#0 8,11

M\_CS3# 7,11

M\_B\_WE# 8,11

M\_B\_CAS# 8,11

RN37

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_A\_A13

M\_ODT0 7,11

M\_CS0# 7,11

M\_A\_RAS# 8,11

RN32

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_A\_BS#1 8,11

M\_A\_A0

M\_A\_A2

M\_A\_A4

RN30

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_A\_BS#0 8,11

M\_A\_WE# 8,11

M\_A\_CAS# 8,11

M\_CS1# 7,11

RN25

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_CKE0 7,11

M\_A\_BS#2 8,11

M\_A\_A8

M\_A\_A12

RN27

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_CKE1 7,11

M\_A\_A6

M\_A\_A7

M\_A\_A11

RN26

1 2 3 4

8 7 6 5

SRN56J-5-GP

M\_A\_A5

M\_A\_A3

M\_A\_A1

M\_A\_A10

Put decap near power(0.9V)  
and pull-up resistor

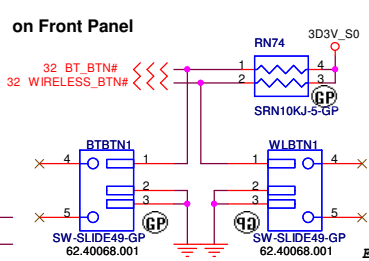
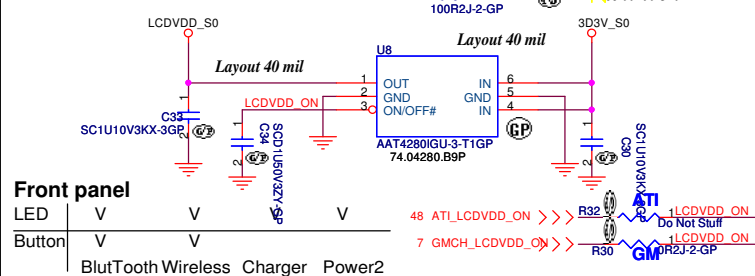
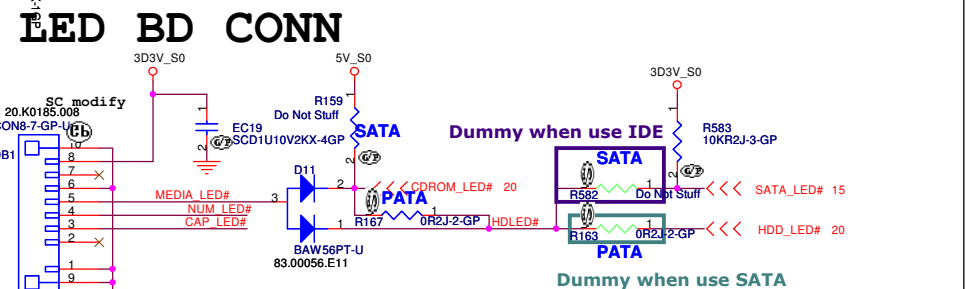
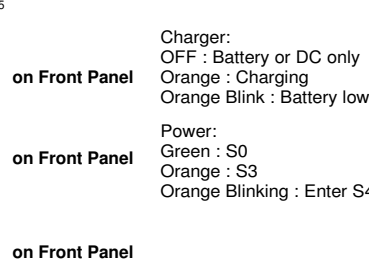
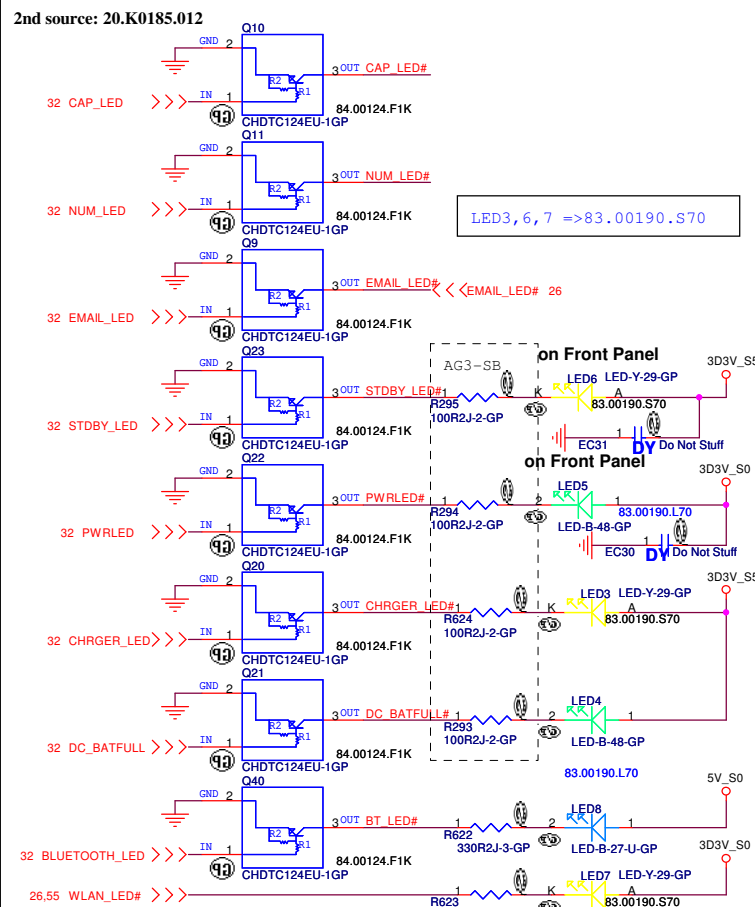
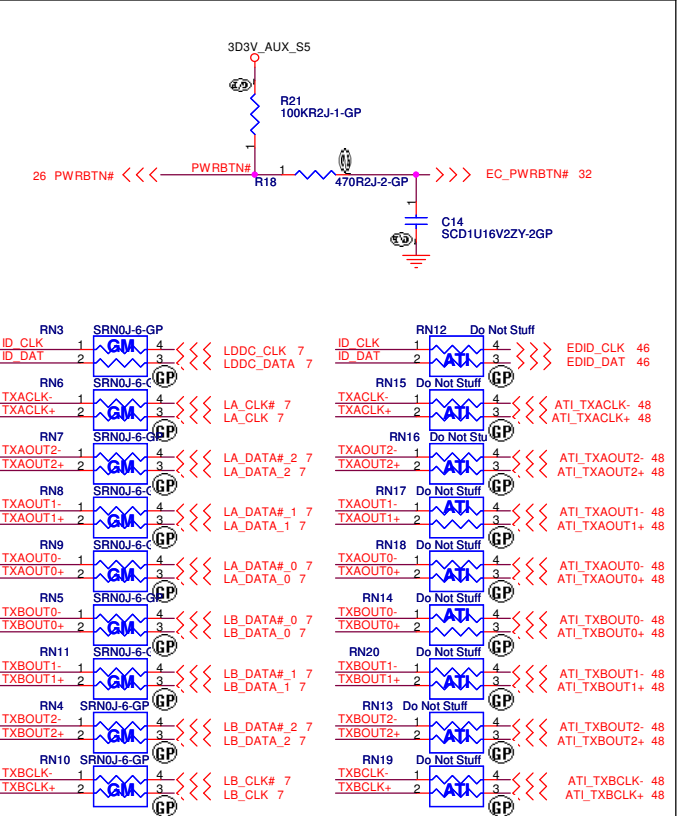
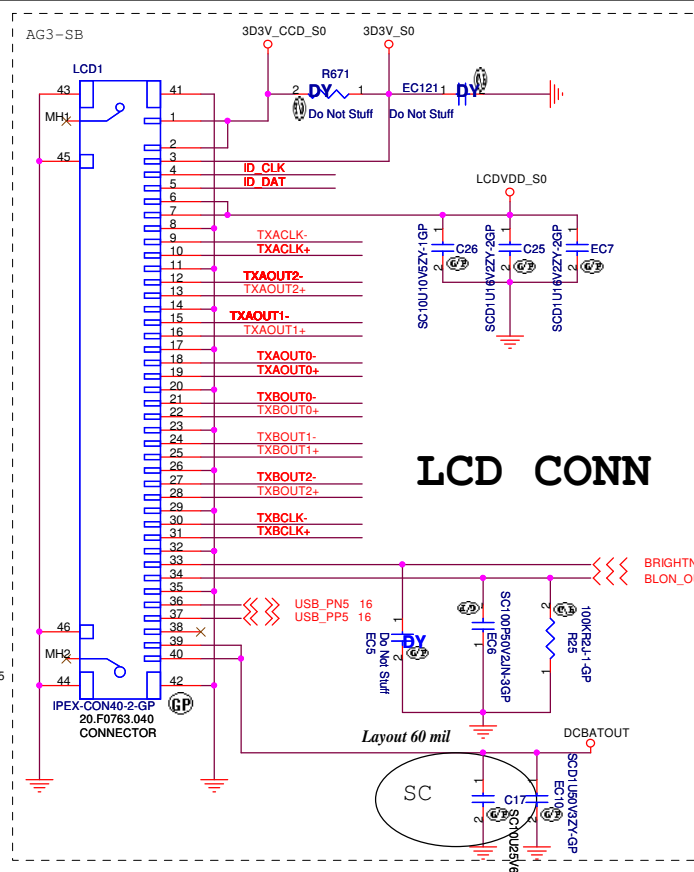
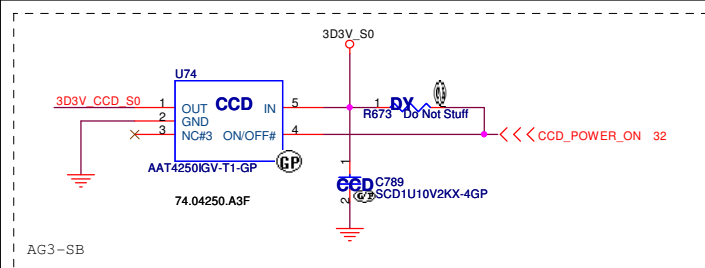
The image shows a detailed PCB layout for the VREF\_S0 signal of a DDR3 memory module. The layout is organized into two rows of components. Each component is labeled with its part number and a reference designator. The components are connected to a common ground plane. The layout includes decoupling capacitors (36pF) and pull-up resistors (2kΩ) for each signal line. The components are arranged in a regular grid pattern, with labels such as C292, C293, C294, C295, C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875, C876, C877, C878, C879, C880, C881, C882, C883, C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C896, C897, C898, C899, C900, C901, C902, C903, C904, C905, C906, C907, C908, C909, C910, C911, C912, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C924, C925, C926, C927, C928, C929, C930, C931, C932, C933, C934, C935, C936, C937, C938, C939, C940, C941, C942, C943, C944, C945, C946, C947, C948, C949, C950, C951, C952, C953, C954, C955, C956, C957, C958, C959, C960, C961, C962, C963, C964, C965, C966, C967, C968, C969, C970, C971, C972, C973, C974, C975, C976, C977, C978, C979, C980, C981, C982, C983, C984, C985, C986, C987, C988, C989, C990, C991, C992, C993, C994, C995, C996, C997, C998, C999, C1000, C1001, C1002, C1003, C1004, C1005, C1006, C1007, C1008, C1009, C1010, C1011, C1012, C1013, C1014, C1015, C1016, C1017, C1018, C1019, C1020, C1021, C1022, C1023, C1024, C1025, C1026, C1027, C1028, C1029, C1030, C1031, C1032, C1033, C1034, C1035, C1036, C1037, C1038, C1039, C1040, C1041, C1042, C1043, C1044, C1045, C1046, C1047, C1048, C1049, C1050, C1051, C1052, C1053, C1054, C1055, C1056, C1057, C1058, C1059, C1060, C1061, C1062, C1063, C1064, C1065, C1066, C1067

The schematic diagram illustrates a four-channel differential amplifier. It features four differential pairs, each consisting of a PMOS load transistor (SC2DUB3/VAMX-1-GP) and an NMOS input transistor (SCD1U6). The gates of the NMOS transistors are biased by a common-mode feedback circuit (C232, C279) and a differential-mode feedback circuit (C212, C234). The output nodes are connected to a common-mode feedback circuit (C232, C279). The circuit is designed for a 1.8V supply and a 100pF load.

The diagram illustrates the correct placement of electrolytic capacitors for several ICs. A 1D8V\_S3 power source is connected to the positive rail. The components and their capacitor placements are as follows:

- SC202A63033MX-1-GP** (Pin 1): Capacitor **C816** (10µF) connected to pins 1 and 2.
- SC202A63033MX-1-GP** (Pin 2): Capacitor **C817** (10µF) connected to pins 2 and 3.
- SC202A63033MX-1-GP** (Pin 3): Capacitor **C818** (10µF) connected to pins 3 and 4.
- SC202A63033MX-1-GP** (Pin 4): Capacitor **C819** (10µF) connected to pins 4 and 5.
- SC202A63033MX-1-GP** (Pin 5): Capacitor **C820** (10µF) connected to pins 5 and 6.
- SC202A63033MX-1-GP** (Pin 6): Capacitor **C821** (10µF) connected to pins 6 and 7.
- SC202A63033MX-1-GP** (Pin 7): Capacitor **C822** (10µF) connected to pins 7 and 8.
- SC202A63033MX-1-GP** (Pin 8): Capacitor **C823** (10µF) connected to pins 8 and 9.
- SC202A63033MX-1-GP** (Pin 9): Capacitor **C824** (10µF) connected to pins 9 and 10.
- SC202A63033MX-1-GP** (Pin 10): Capacitor **C825** (10µF) connected to pins 10 and 11.
- SC202A63033MX-1-GP** (Pin 11): Capacitor **C826** (10µF) connected to pins 11 and 12.
- SC202A63033MX-1-GP** (Pin 12): Capacitor **C827** (10µF) connected to pins 12 and 13.
- SC202A63033MX-1-GP** (Pin 13): Capacitor **C828** (10µF) connected to pins 13 and 14.
- SC202A63033MX-1-GP** (Pin 14): Capacitor **C829** (10µF) connected to pins 14 and 15.
- SC202A63033MX-1-GP** (Pin 15): Capacitor **C830** (10µF) connected to pins 15 and 16.
- SC202A63033MX-1-GP** (Pin 16): Capacitor **C831** (10µF) connected to pins 16 and 17.
- SC202A63033MX-1-GP** (Pin 17): Capacitor **C832** (10µF) connected to pins 17 and 18.
- SC202A63033MX-1-GP** (Pin 18): Capacitor **C833** (10µF) connected to pins 18 and 19.
- SC202A63033MX-1-GP** (Pin 19): Capacitor **C834** (10µF) connected to pins 19 and 20.
- SC202A63033MX-1-GP** (Pin 20): Capacitor **C835** (10µF) connected to pins 20 and 21.
- SC202A63033MX-1-GP** (Pin 21): Capacitor **C836** (10µF) connected to pins 21 and 22.
- SC202A63033MX-1-GP** (Pin 22): Capacitor **C837** (10µF) connected to pins 22 and 23.
- SC202A63033MX-1-GP** (Pin 23): Capacitor **C838** (10µF) connected to pins 23 and 24.
- SC202A63033MX-1-GP** (Pin 24): Capacitor **C839** (10µF) connected to pins 24 and 25.
- SC202A63033MX-1-GP** (Pin 25): Capacitor **C840** (10µF) connected to pins 25 and 26.
- SC202A63033MX-1-GP** (Pin 26): Capacitor **C841** (10µF) connected to pins 26 and 27.
- SC202A63033MX-1-GP** (Pin 27): Capacitor **C842** (10µF) connected to pins 27 and 28.
- SC202A63033MX-1-GP** (Pin 28): Capacitor **C843** (10µF) connected to pins 28 and 29.
- SC202A63033MX-1-GP** (Pin 29): Capacitor **C844** (10µF) connected to pins 29 and 30.
- SC202A63033MX-1-GP** (Pin 30): Capacitor **C845** (10µF) connected to pins 30 and 31.
- SC202A63033MX-1-GP** (Pin 31): Capacitor **C846** (10µF) connected to pins 31 and 32.
- SC202A63033MX-1-GP** (Pin 32): Capacitor **C847** (10µF) connected to pins 32 and 33.
- SC202A63033MX-1-GP** (Pin 33): Capacitor **C848** (10µF) connected to pins 33 and 34.
- SC202A63033MX-1-GP** (Pin 34): Capacitor **C849** (10µF) connected to pins 34 and 35.
- SC202A63033MX-1-GP** (Pin 35): Capacitor **C850** (10µF) connected to pins 35 and 36.
- SC202A63033MX-1-GP** (Pin 36): Capacitor **C851** (10µF) connected to pins 36 and 37.
- SC202A63033MX-1-GP** (Pin 37): Capacitor **C852** (10µF) connected to pins 37 and 38.
- SC202A63033MX-1-GP** (Pin 38): Capacitor **C853** (10µF) connected to pins 38 and 39.
- SC202A63033MX-1-GP** (Pin 39): Capacitor **C854** (10µF) connected to pins 39 and 40.
- SC202A63033MX-1-GP** (Pin 40): Capacitor **C855** (10µF) connected to pins 40 and 41.
- SC202A63033MX-1-GP** (Pin 41): Capacitor **C856** (10µF) connected to pins 41 and 42.
- SC202A63033MX-1-GP** (Pin 42): Capacitor **C857** (10µF) connected to pins 42 and 43.
- SC202A63033MX-1-GP** (Pin 43): Capacitor **C858** (10µF) connected to pins 43 and 44.
- SC202A63033MX-1-GP** (Pin 44): Capacitor **C859** (10µF) connected to pins 44 and 45.
- SC202A63033MX-1-GP** (Pin 45): Capacitor **C860** (10µF) connected to pins 45 and 46.
- SC202A63033MX-1-GP** (Pin 46): Capacitor **C861** (10µF) connected to pins 46 and 47.
- SC202A63033MX-1-GP** (Pin 47): Capacitor **C862** (10µF) connected to pins 47 and 48.
- SC202A63033MX-1-GP** (Pin 48): Capacitor **C863** (10µF) connected to pins 48 and 49.
- SC202A63033MX-1-GP** (Pin 49): Capacitor **C864** (10µF) connected to pins 49 and 50.
- SC202A63033MX-1-GP** (Pin 50): Capacitor **C865** (10µF) connected to pins 50 and 51.
- SC202A63033MX-1-GP** (Pin 51): Capacitor **C866** (10µF) connected to pins 51 and 52.
- SC202A63033MX-1-GP** (Pin 52): Capacitor **C867** (10µF) connected to pins 52 and 53.
- SC202A63033MX-1-GP** (Pin 53): Capacitor **C868** (10µF) connected to pins 53 and 54.
- SC202A63033MX-1-GP** (Pin 54): Capacitor **C869** (10µF) connected to pins 54 and 55.
- SC202A63033MX-1-GP** (Pin 55): Capacitor **C870** (10µF) connected to pins 55 and 56.
- SC202A63033MX-1-GP** (Pin 56): Capacitor **C871** (10µF) connected to pins 56 and 57.
- SC202A63033MX-1-GP** (Pin 57): Capacitor **C872** (10µF) connected to pins 57 and 58.
- SC202A63033MX-1-GP** (Pin 58): Capacitor **C873** (10µF) connected to pins 58 and 59.
- SC202A63033MX-1-GP** (Pin 59): Capacitor **C874** (10µF) connected to pins 59 and 60.
- SC202A63033MX-1-GP** (Pin 60): Capacitor **C875** (10µF) connected to pins 60 and 61.
- SC202A63033MX-1-GP** (Pin 61): Capacitor **C876** (10µF) connected to pins 61 and 62.
- SC202A63033MX-1-GP** (Pin 62): Capacitor **C877** (10µF) connected to pins 62 and 63.
- SC202A63033MX-1-GP** (Pin 63): Capacitor **C878** (10µF) connected to pins 63 and 64.
- SC202A63033MX-1-GP** (Pin 64): Capacitor **C879** (10µF) connected to pins 64 and 65.
- SC202A63033MX-1-GP** (Pin 65): Capacitor **C880** (10µF) connected to pins 65 and 66.
- SC202A63033MX-1-GP** (Pin 66): Capacitor **C881** (10µF) connected to pins 66 and 67.
- SC202A63033MX-1-GP** (Pin 67): Capacitor **C882** (10µF) connected to pins 67 and 68.
- SC202A63033MX-1-GP** (Pin 68): Capacitor **C883** (10µF) connected to pins 68 and 69.
- SC202A63033MX-1-GP** (Pin 69): Capacitor **C88**

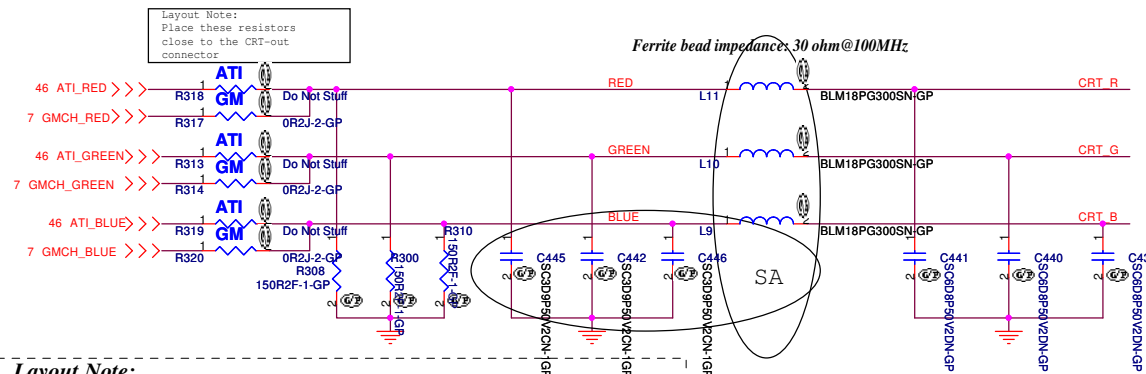
Title			
<b>DDR2 Termination Resistor</b>			
Size A3	Document Number		Rev
	<b>AG3</b>		<b>2</b>
Date:	Friday, April 21, 2006	Sheet 12 of	55



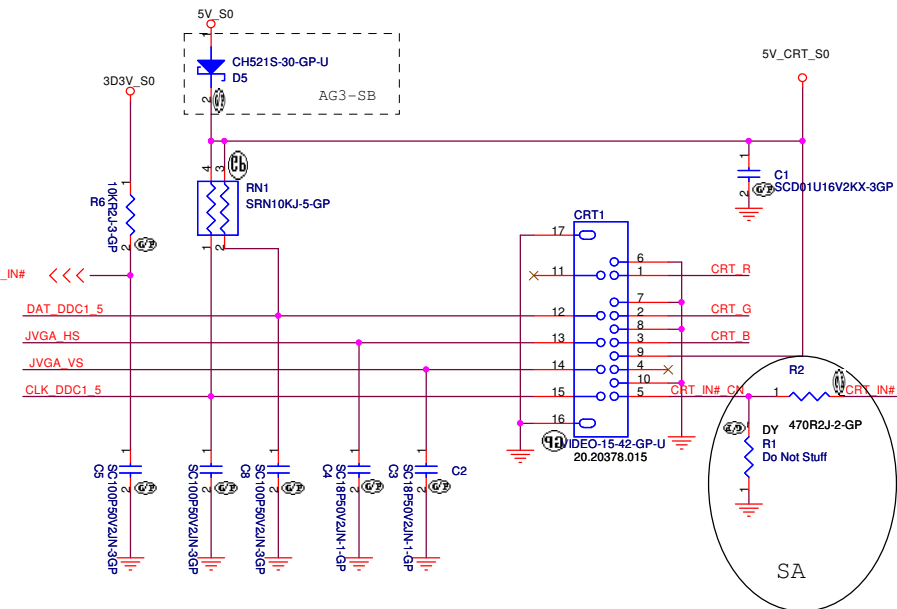


# CRT I/F & CONNECTOR

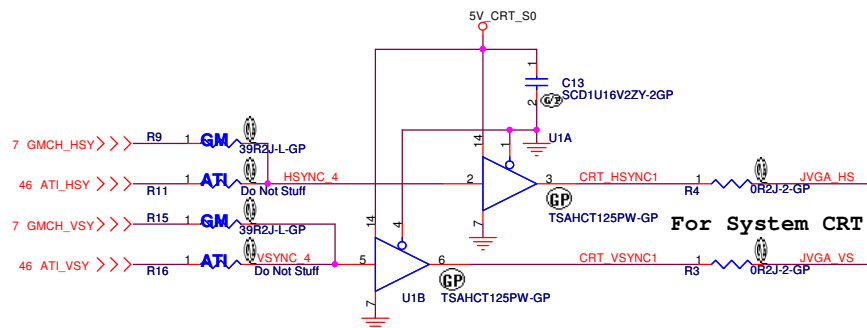
Ferrite bead impedances 30 ohm@100MHz



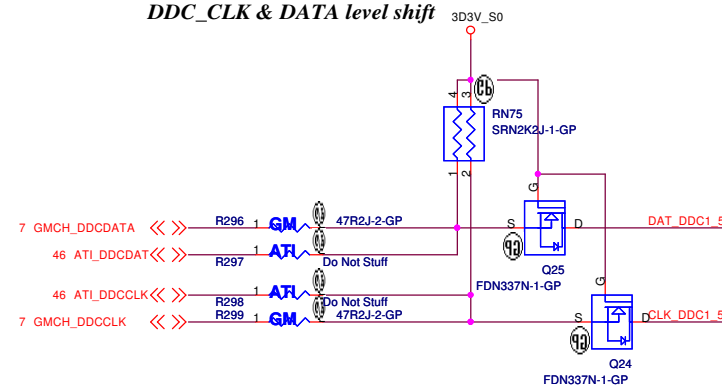
**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



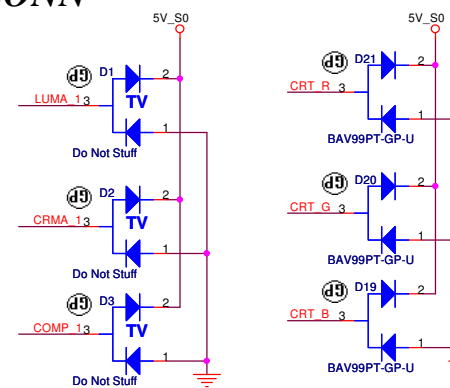
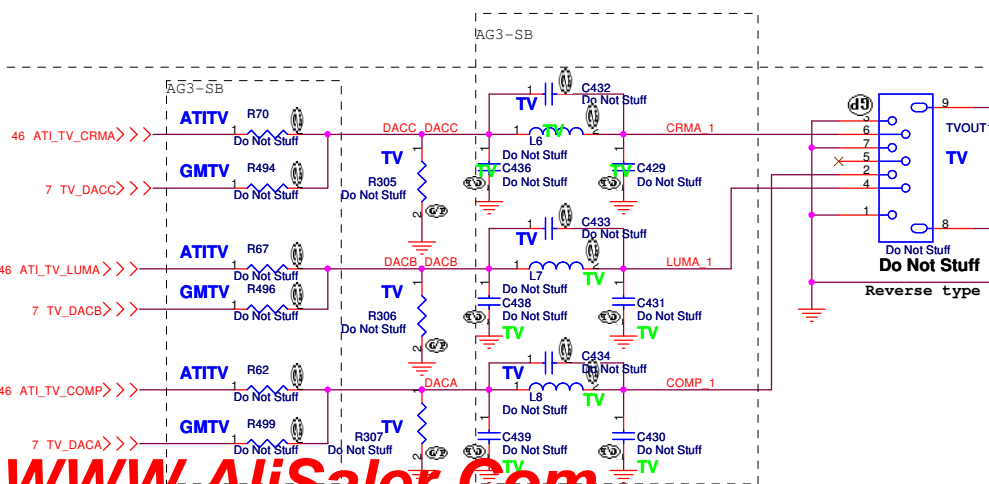
## Hsync & Vsync level shift



## DDC\_CLK & DATA level shift



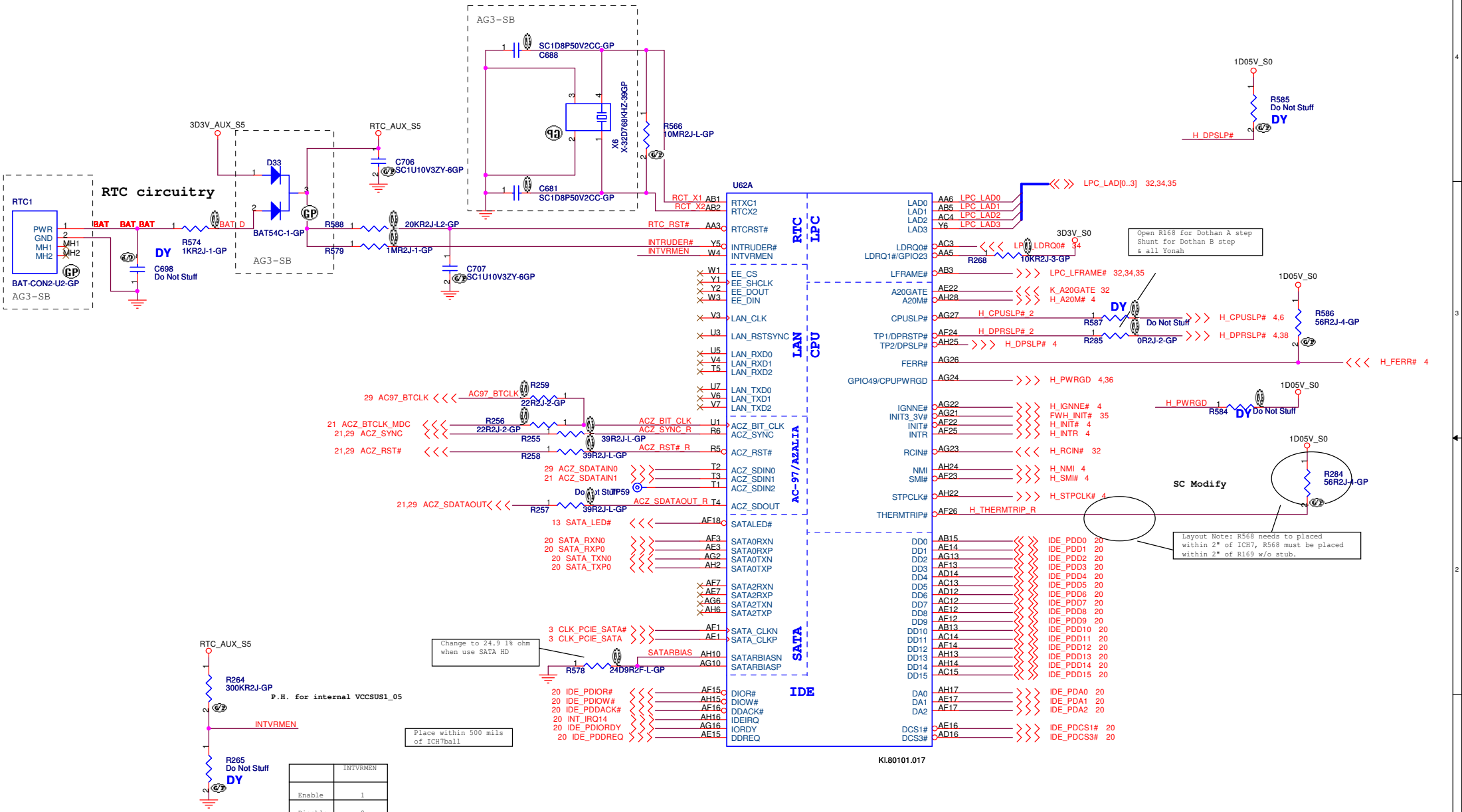
## TV OUT CONN



BOM

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

CRT/TV Connector			
Size A3	Document Number	AG3	Rev 2
Date: Thursday, April 20, 2006	Sheet 14	of 55	



Placement Note:  
Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

	INTVRMEN
Enable	1
Disable	0

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

ICH7-M (1 of 4)

Size

A3

Document Number

AG3

Date

Friday, April 21, 2006

Sheet

15

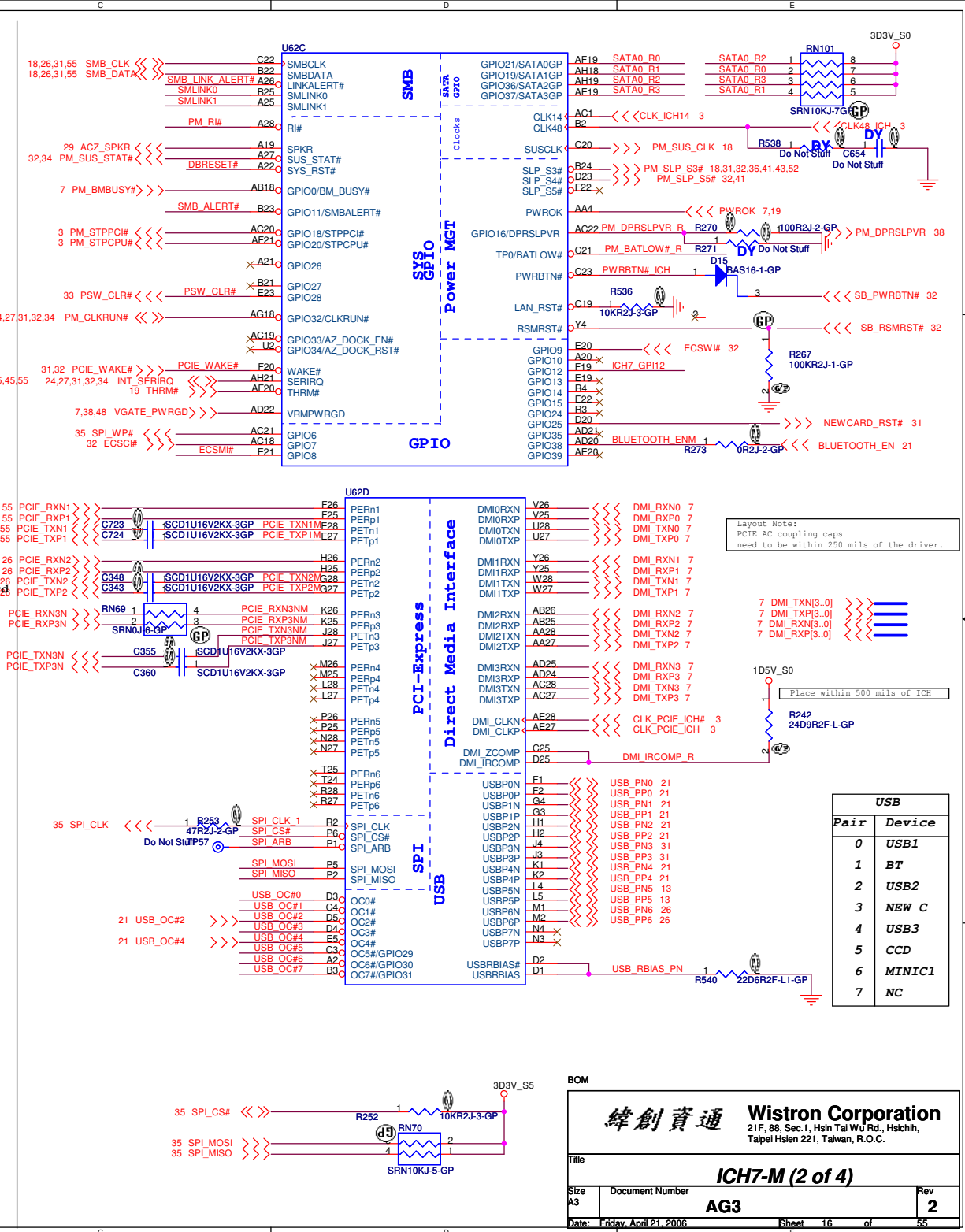
of

55

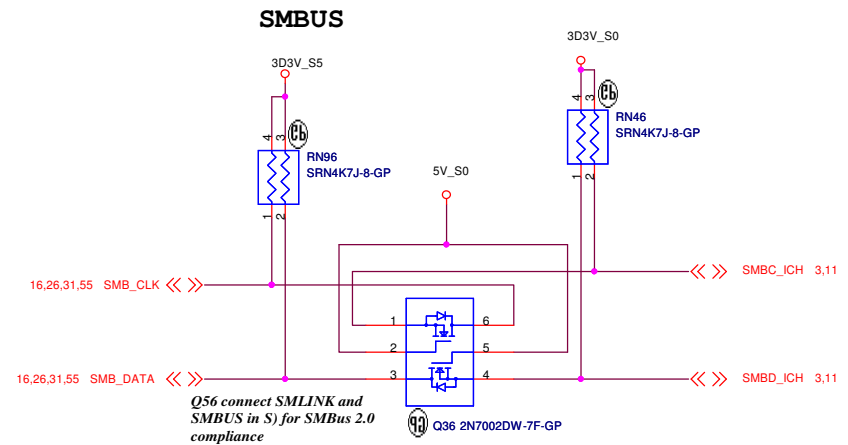
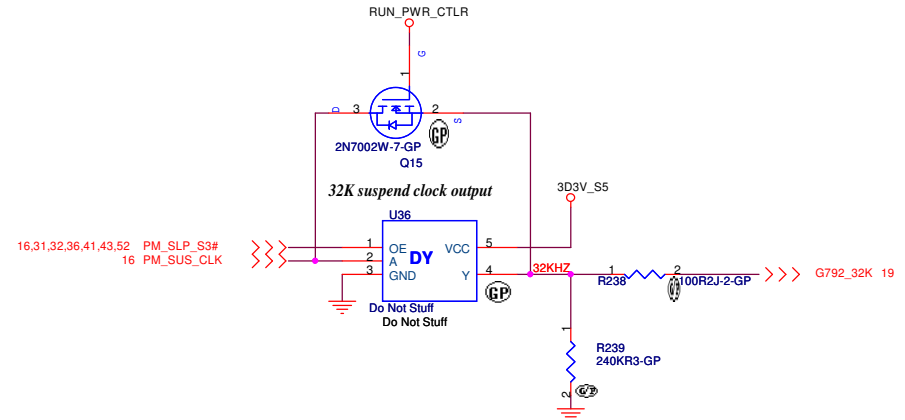
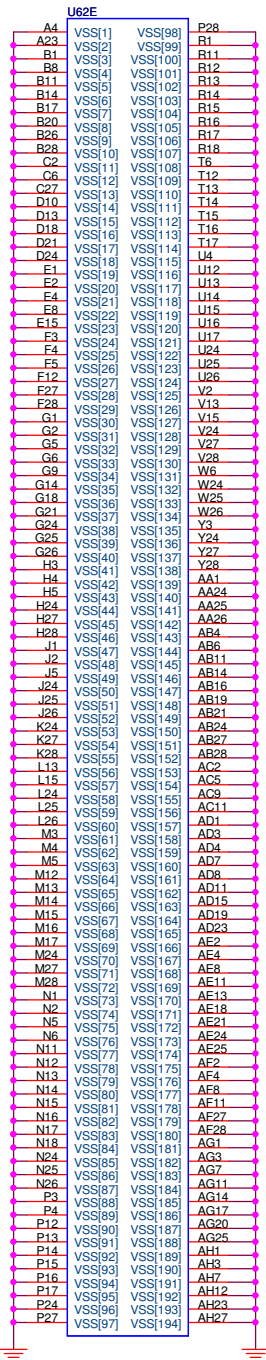
Rev

2

K1.80101.017





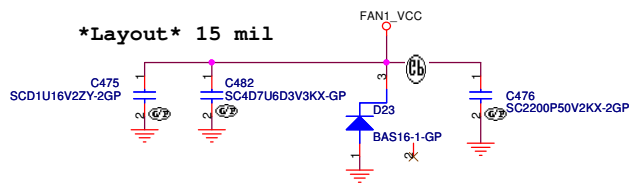


BOM

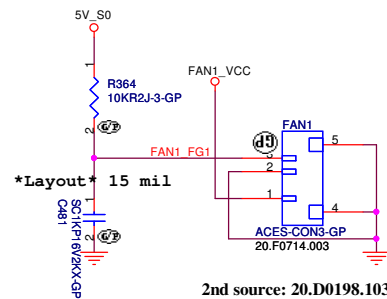
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
<b>ICH7-M (4 of 4)</b>			
Size A3	Document Number	Rev 2	
Date: Friday, April 21, 2006		Sheet 18	of 55



**\*Layout\* 15 mil**

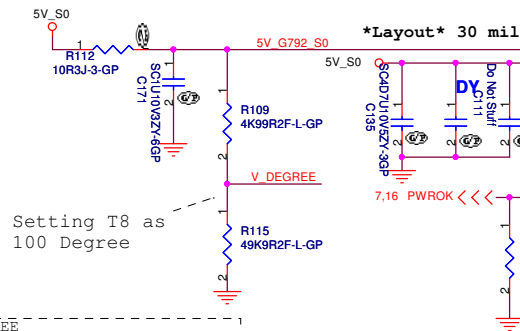
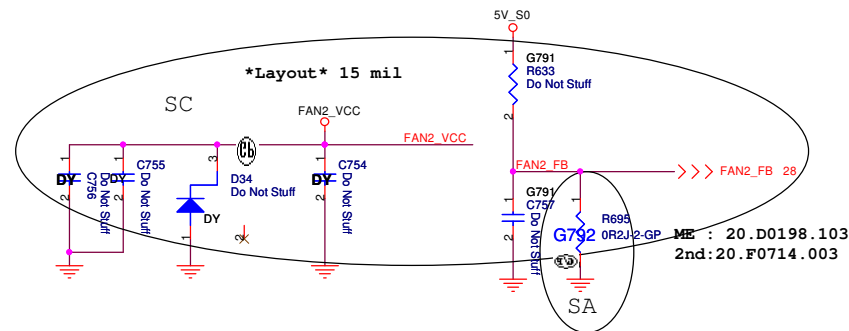


**\*Layout\* 15 mil**



2nd source: 20.D0198.103

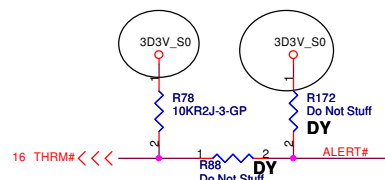
**\*Layout\* 15 mil**



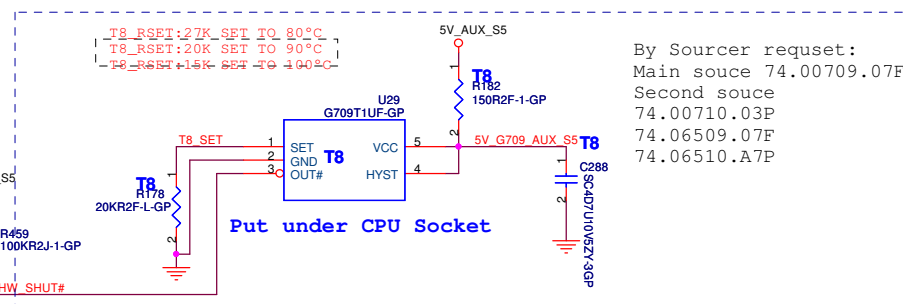
Setting T8 as  
100 Degree

V\_DEGREE  
= (((Degree-72)\*0.02)+0.34)\*VCC  
HW thermal shut down temperature  
setting 95 degree . Put Near CPU .

DXP1:108 Degree  
DXP2:H/W Setting  
DXP3:88 Degree



32.36 PURE\_HW\_SHUTDOWN# <<<



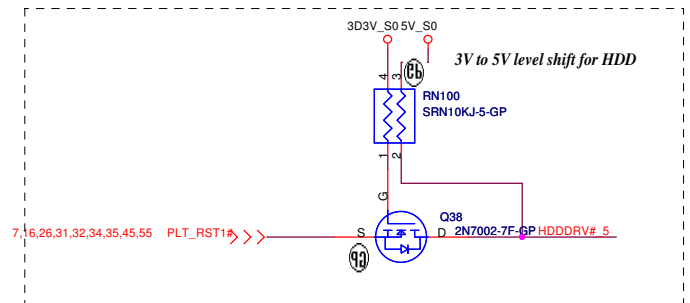
Put under CPU Socket

By Sourcer request:  
Main souce 74.00709.07F  
Second souce  
74.00710.03P  
74.06509.07F  
74.06510.A7P

BOM

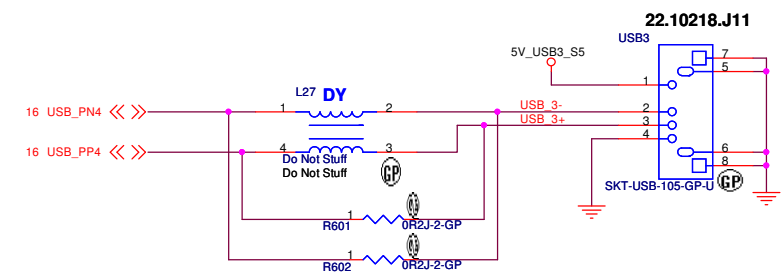
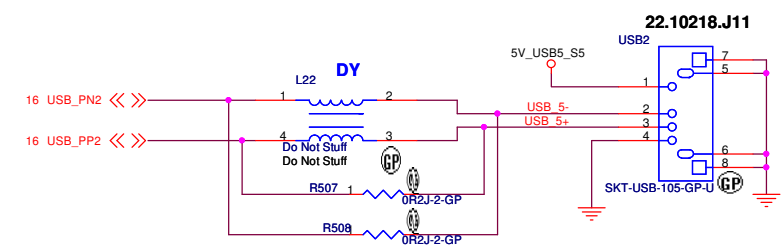
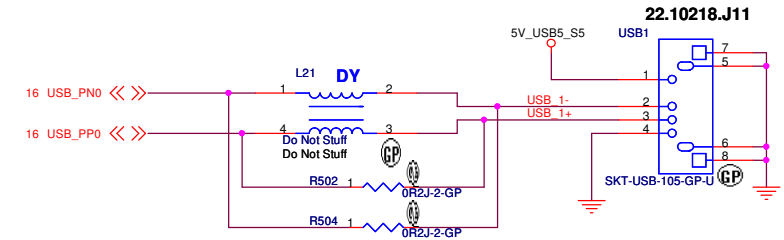
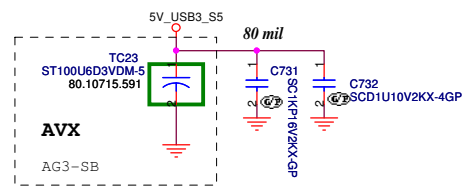
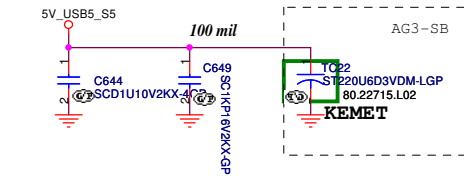
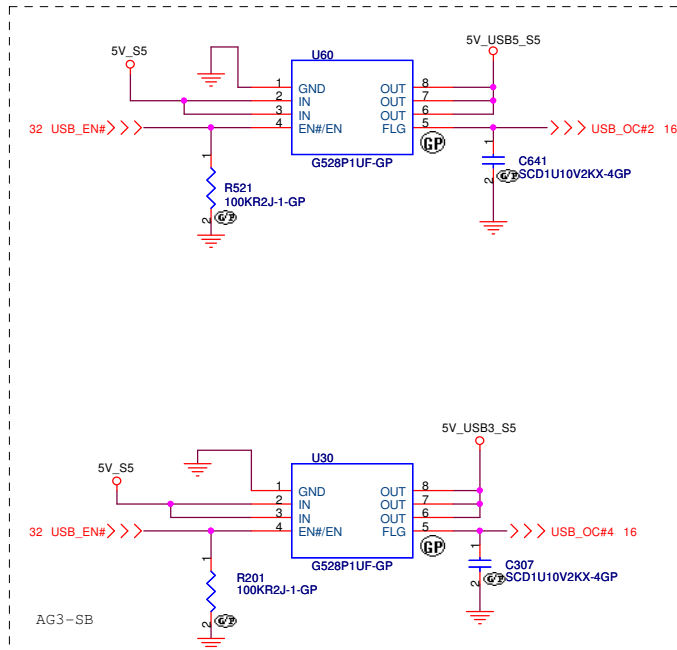
<b>緯創資通</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
<b>Thermal/Fan Controller G792</b>		Size A3	
Date: Friday, April 21, 2006		Document Number	
Sheet 19 of 55		Rev 2	

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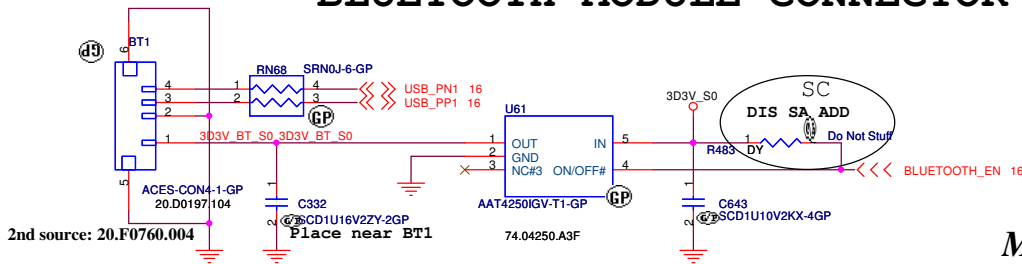


Title				<b>SATA/PATA HDD / ODD</b>			
Size A3		Document Number				Rev	
		<b>AG3</b>				<b>2</b>	
Date: Thursday, April 20, 2006				Sheet 20 of		55	

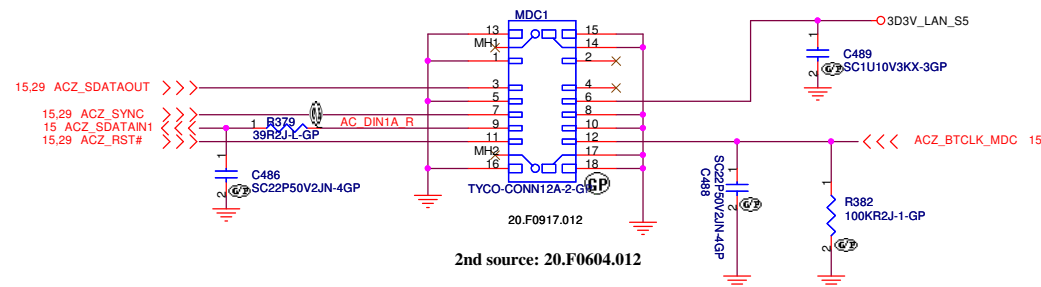
# USB PORT



## BLUETOOTH MODULE CONNECTOR



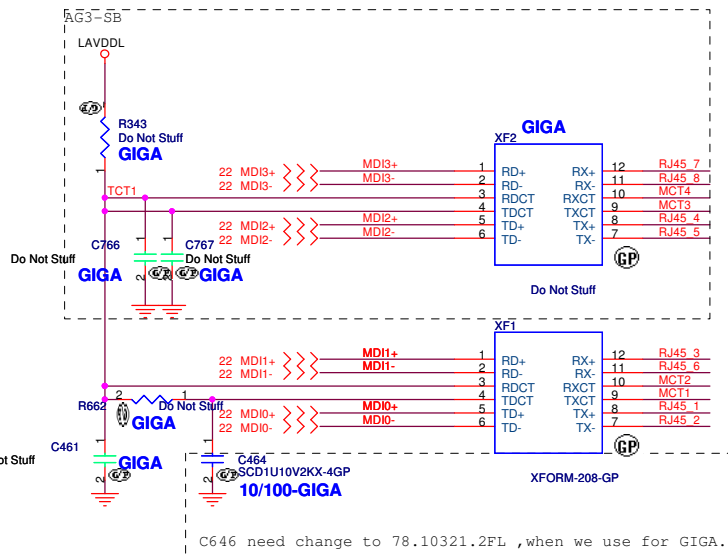
## MDC 1.5 CONN



BOM			
<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB and MDC I/F</b>			
Size A3	Document Number <b>AG3</b>	Rev <b>2</b>	
Date: Friday, April 21, 2006	Sheet 21	of	55

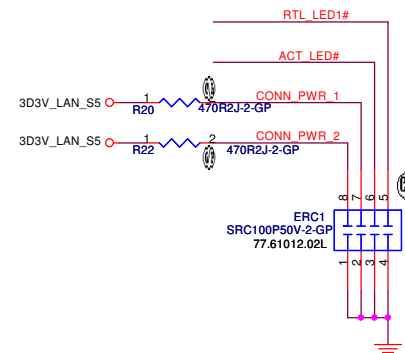
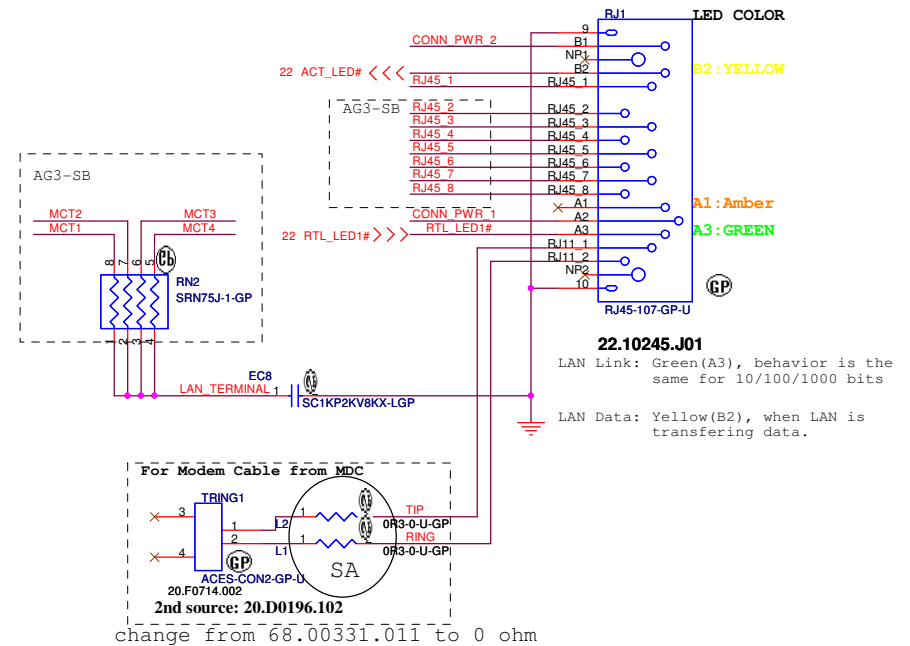


PIN NAME	8110SBL (Giga)	8100CL (10/100)	SIGNAL NAME
VDD33	3.3	3.3	3D3V_LAN_S5
AVDDH	3.3	N.C.	AVDDH
VDD18	1.2	2.5	DVDD
AVDD18	1.2	2.5	DVDD_A
AVDDL	2.5	3.3	AVDDL
V_12P	3.3	2.5	V_12P



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

## LAN Connector



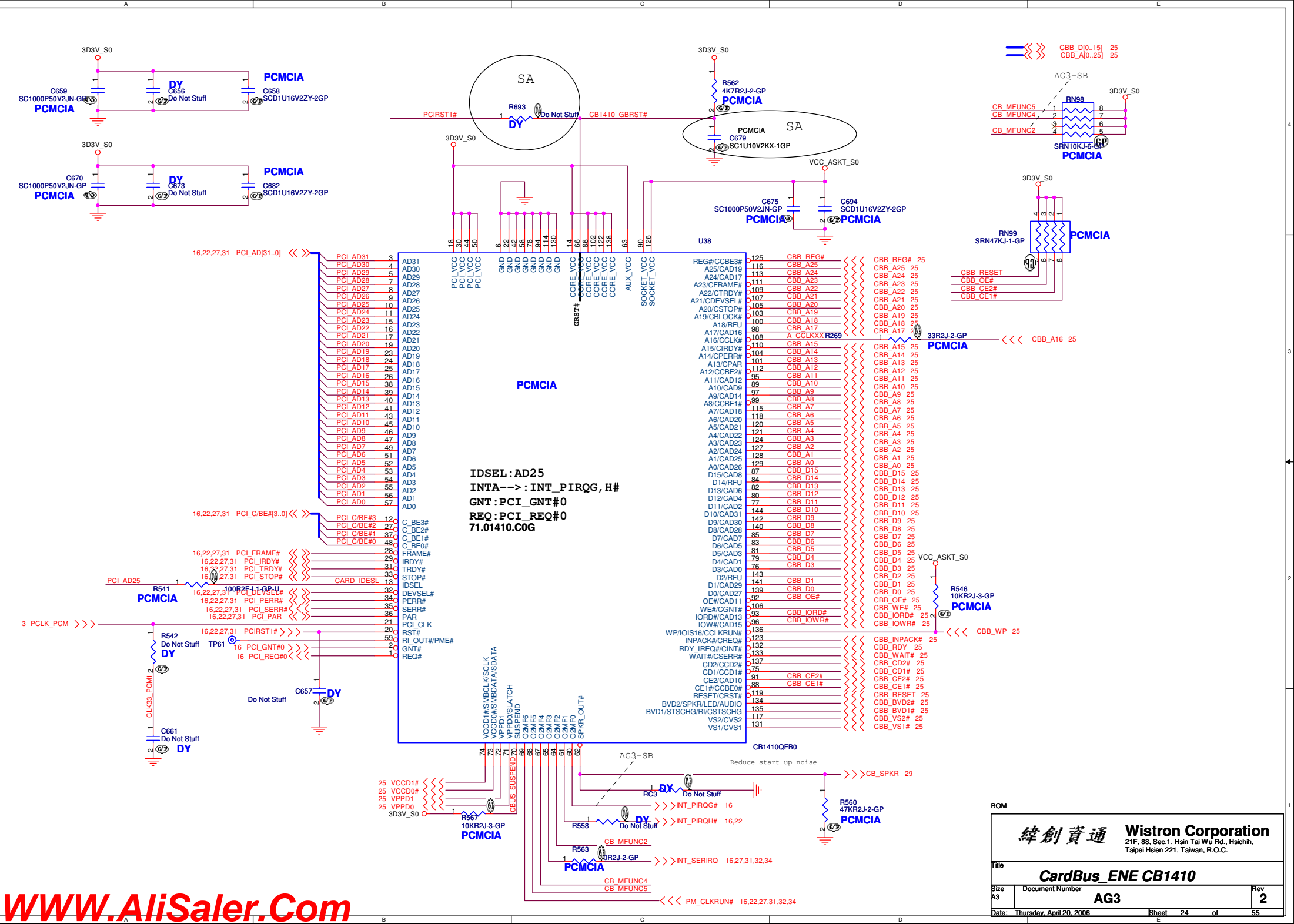
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

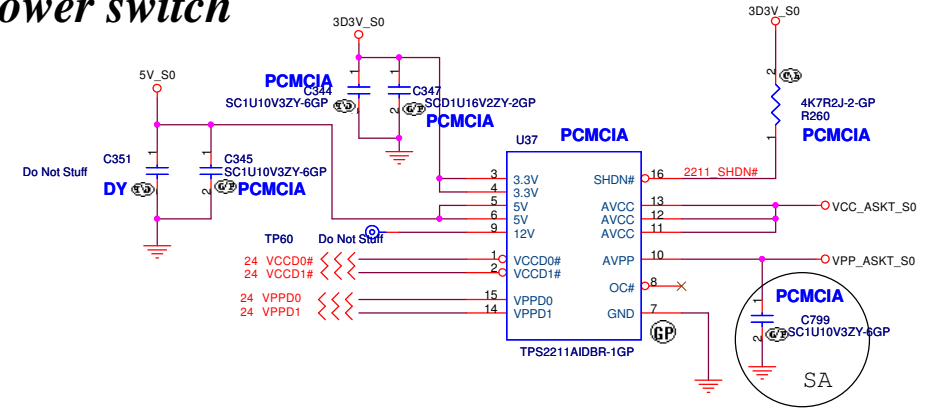
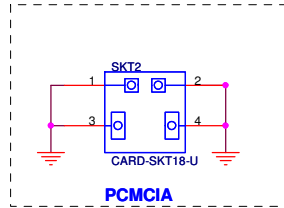
Size A3 Document Number **AG3** Rev **2**

Date: Thursday, April 20, 2006 Sheet 23 of 55

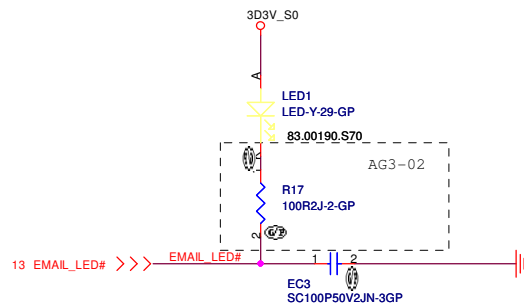
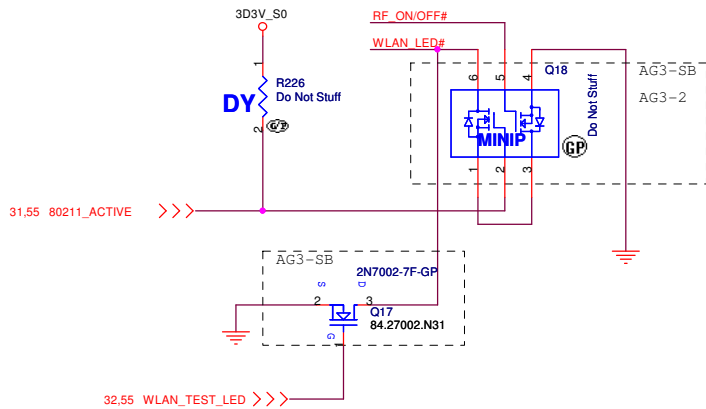
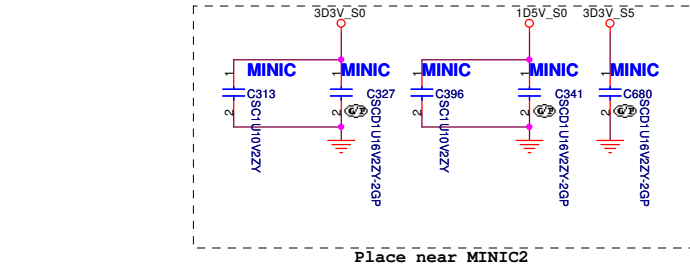
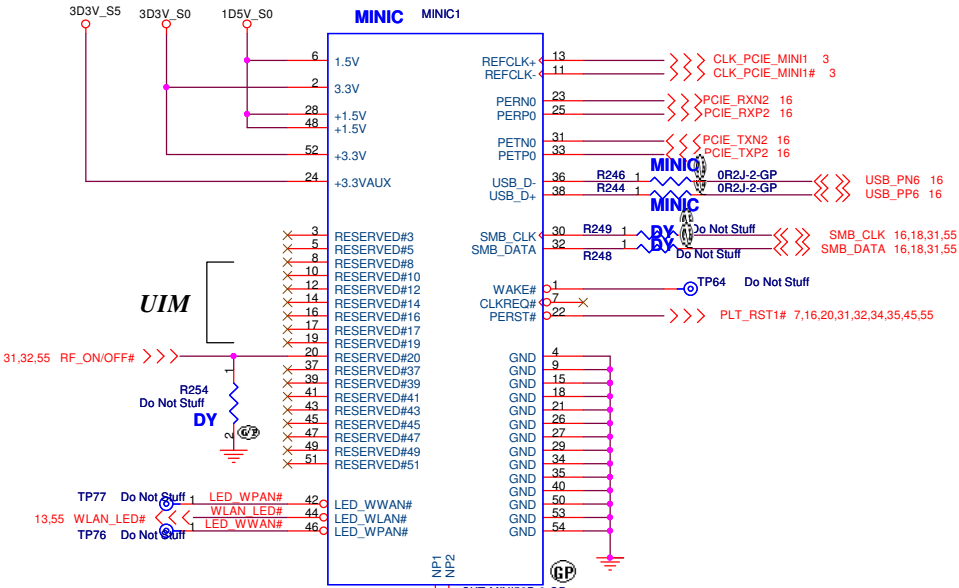




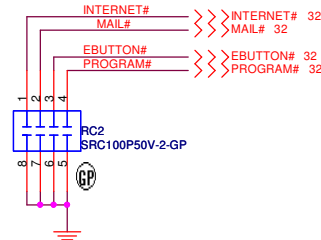
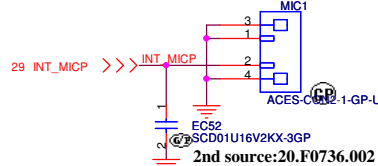
### *Power switch*



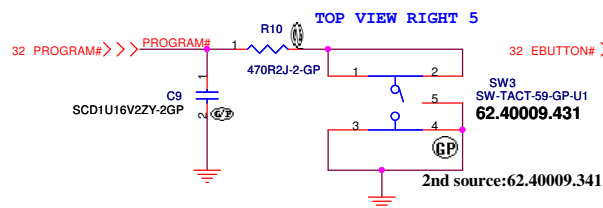
# Mini Card Connector



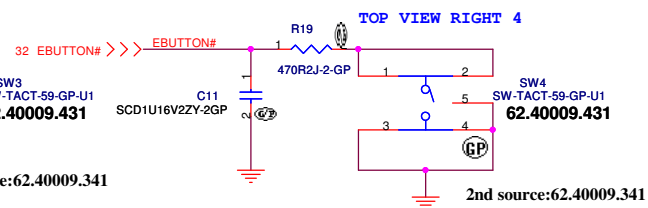
## Internal Microphone



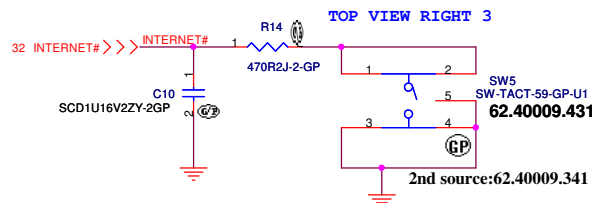
## Program Button



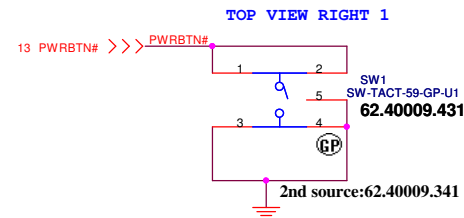
## E-Button



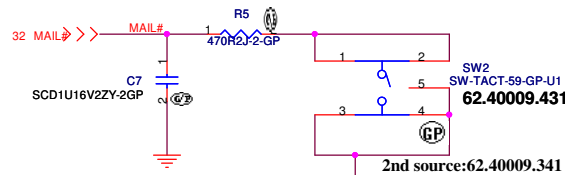
## Internet Button



## Power Button



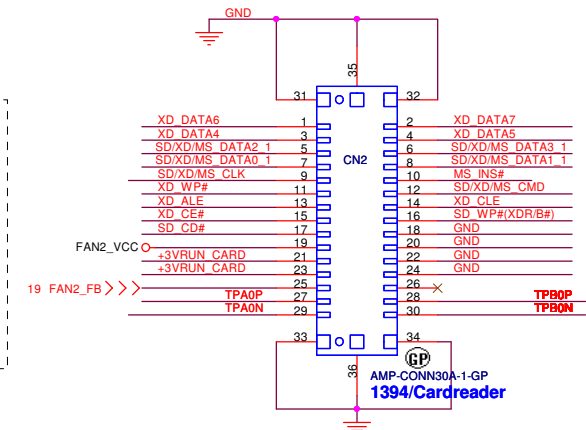
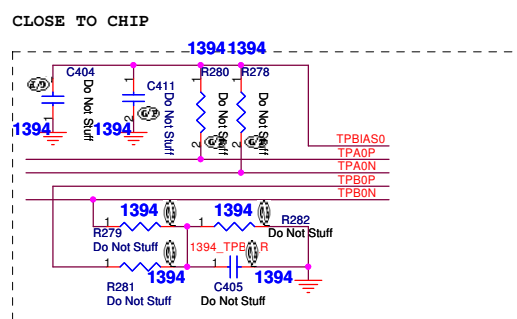
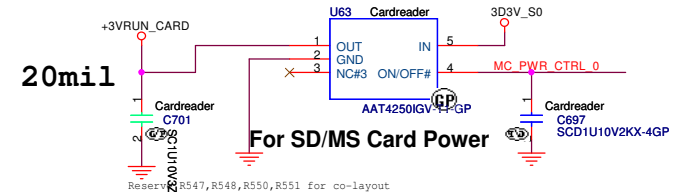
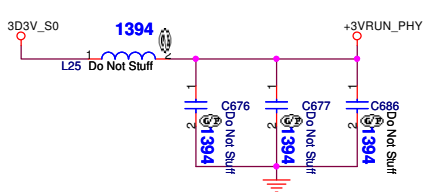
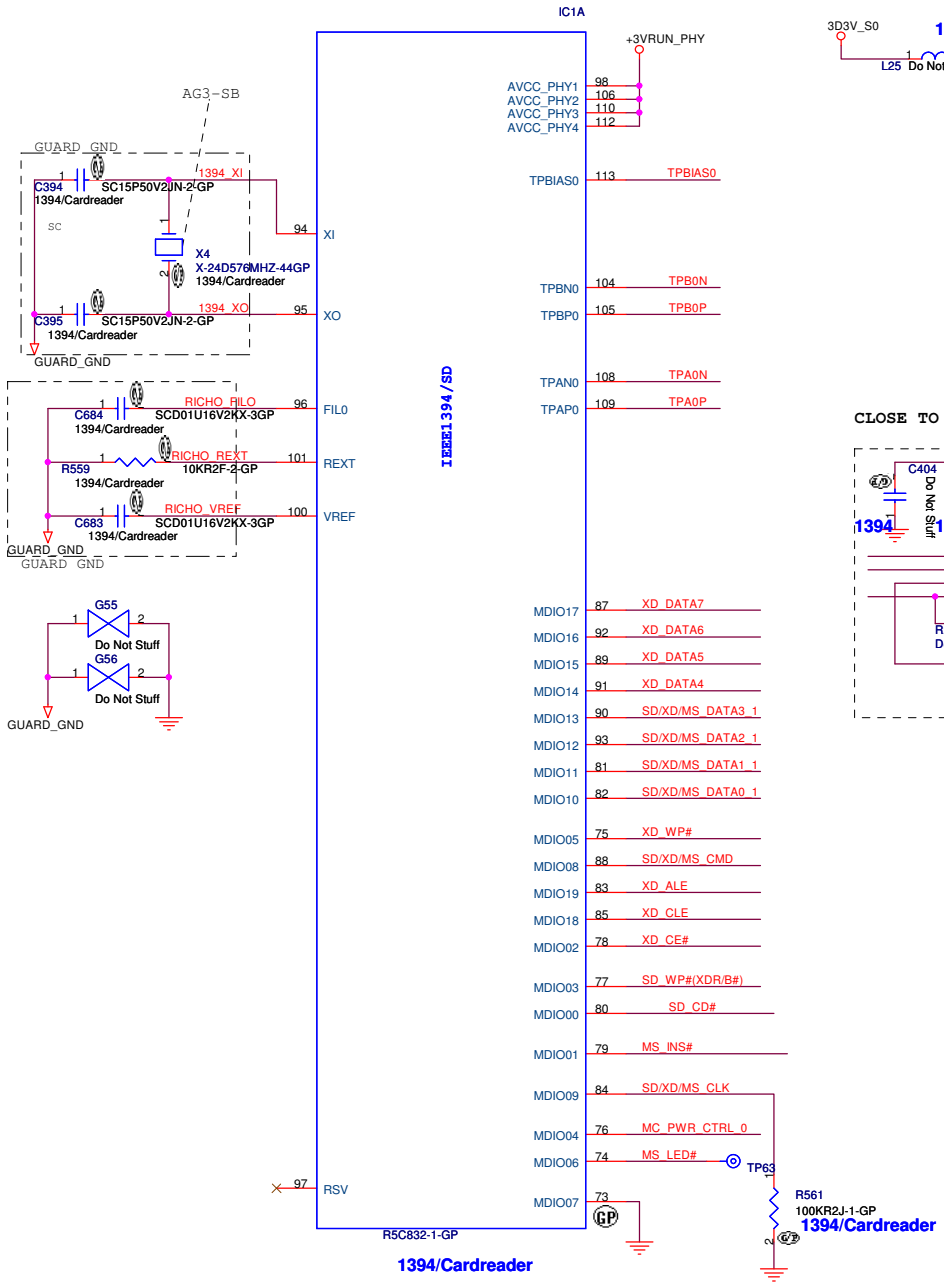
## Mail Button



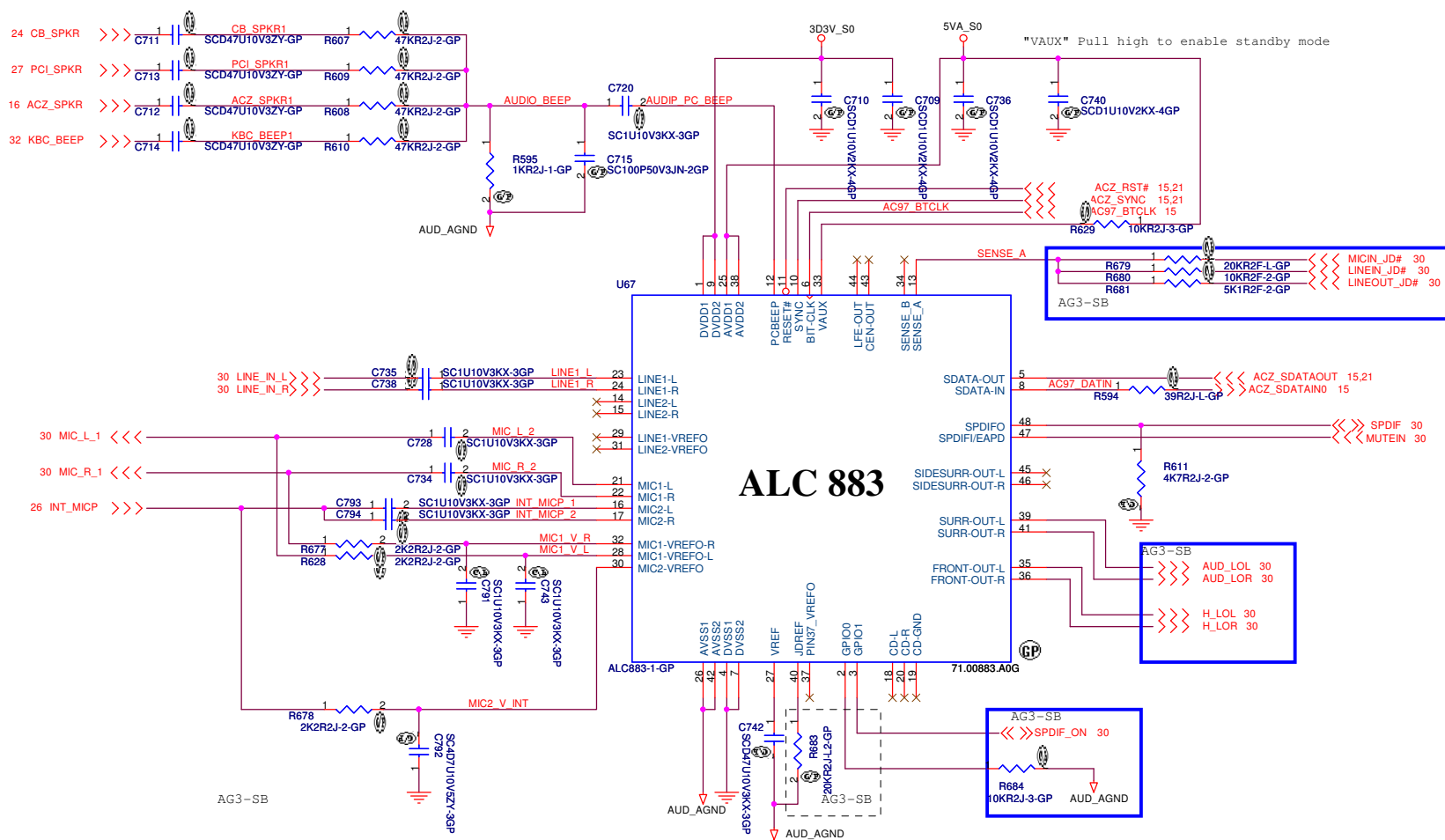
BOM

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>MINI CARD / Button</b>		
Size A3	Document Number	Rev 2
Date: Wednesday, April 26, 2006 Sheet 26 of 55		





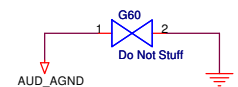
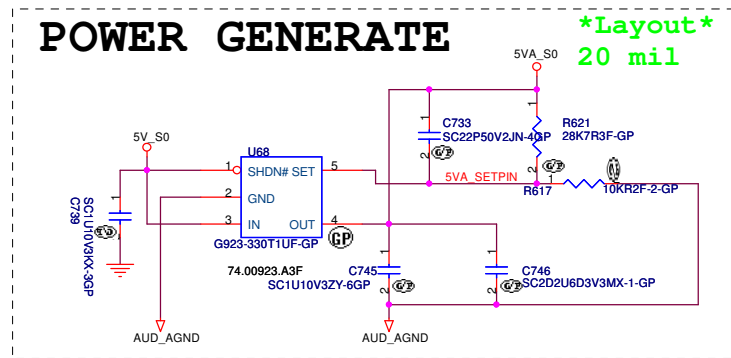




1) When GPIO0 is asserted, AMP should be muted.  
 2) SPDIFO should be turned off when not used.

**Configuration:**  
 (3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

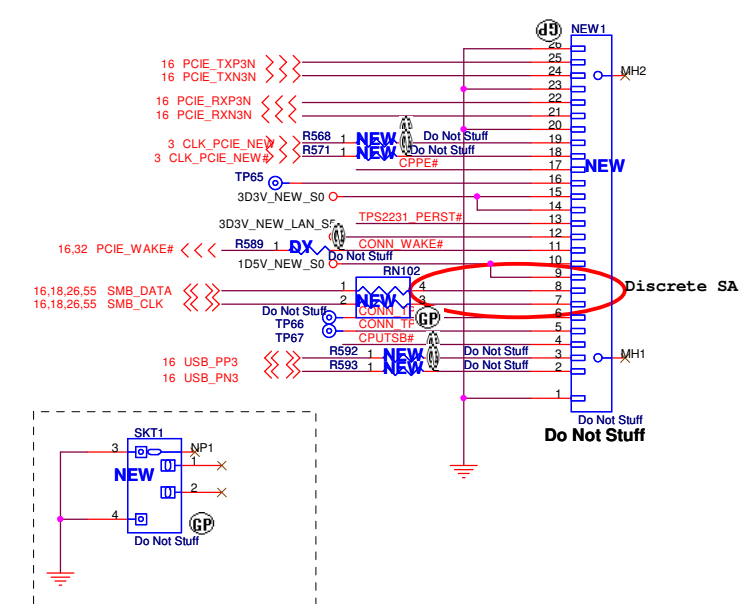
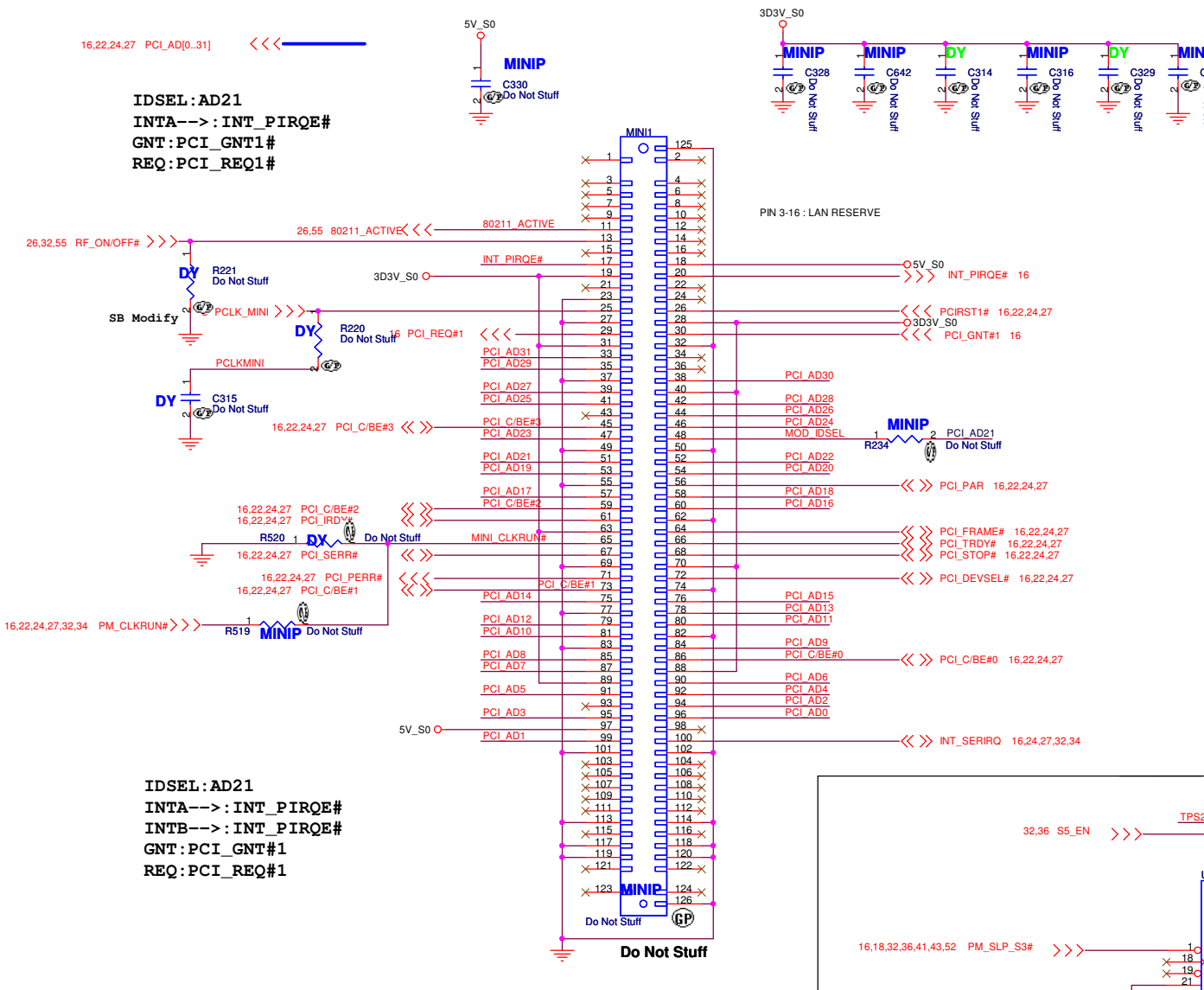
Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP, Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREF0-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREF0-R, SIDESURR-R is LINE2-VREF0-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



BOM

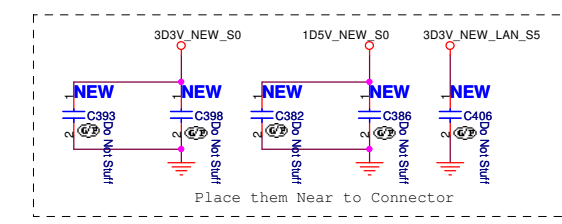
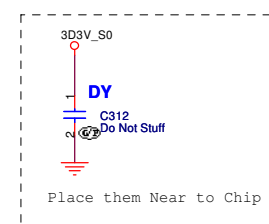
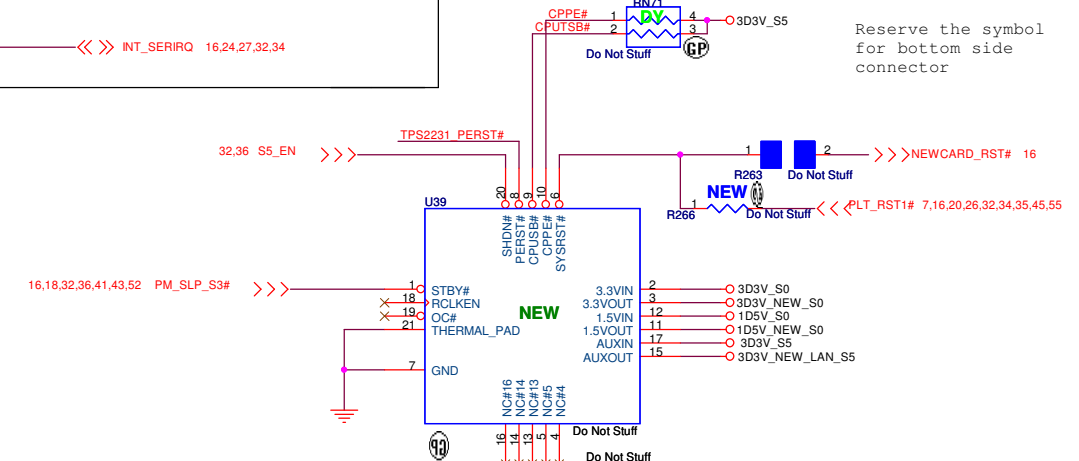
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title Azalia codec ALC883</b>	
Size A3 Document Number <b>AG3</b>	Rev <b>2</b>
Date: Thursday, April 20, 2006 Sheet 29 of 55	





## NEWCARD Connector

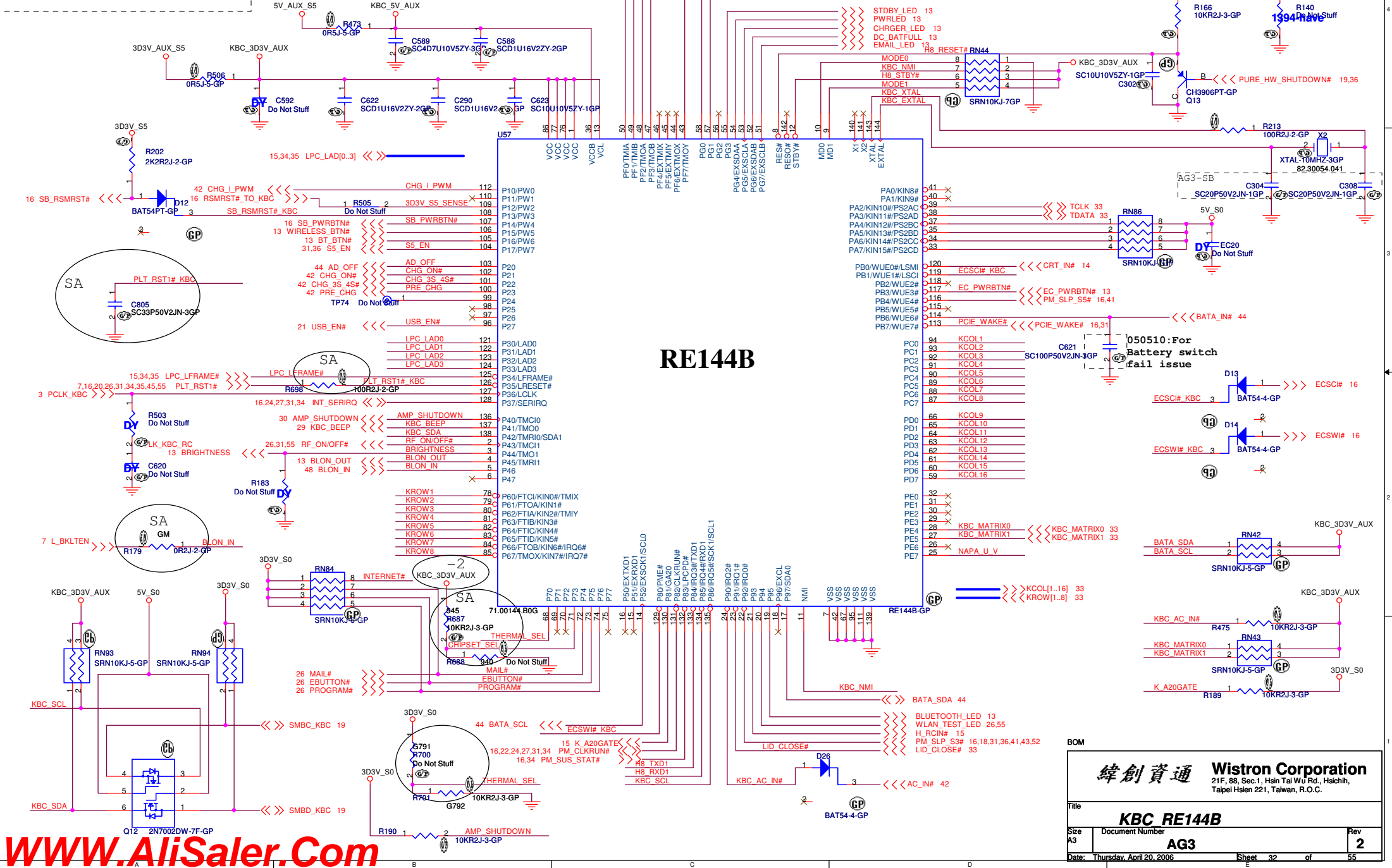
Reserve the symbol  
for bottom side  
connector



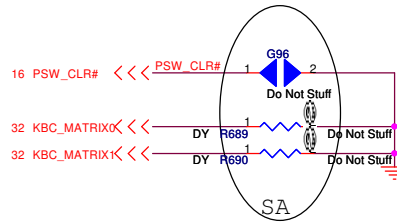
BOM		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
File <b>MINI-PCI/NEW Card</b>		
Size A3	Document Number <b>AG3</b>	Rev <b>2</b>
Date: Thursday, April 20, 2006		Sheet 31 of 55

# For S/W Debug

Pin No.			Pin No.
1	3D3V_AUX_KBC		
		TP24	MODE1
3	H8 RESET#	TP48	MODE0
		TP31	
5	KBC_AC_IN#	TP73	H8_TXD1
		TP29	
7	LID_CLOSE#	TP19	H8_RXD1
		TP36	
9	PM_SLP_S3#	TP20	GND
			10

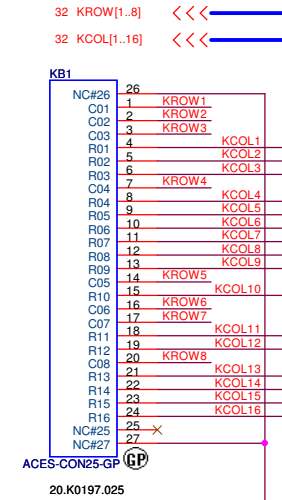


## Internal KeyBoard Connector

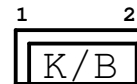


Keyboard matrix ( from vendor )

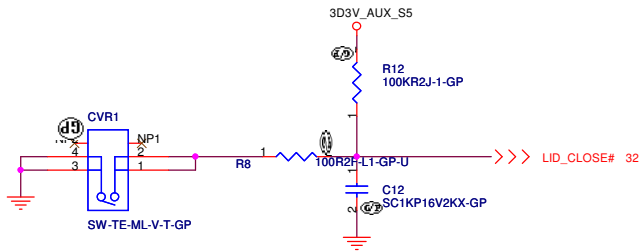
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0



**2nd source: 20.K0198.025**

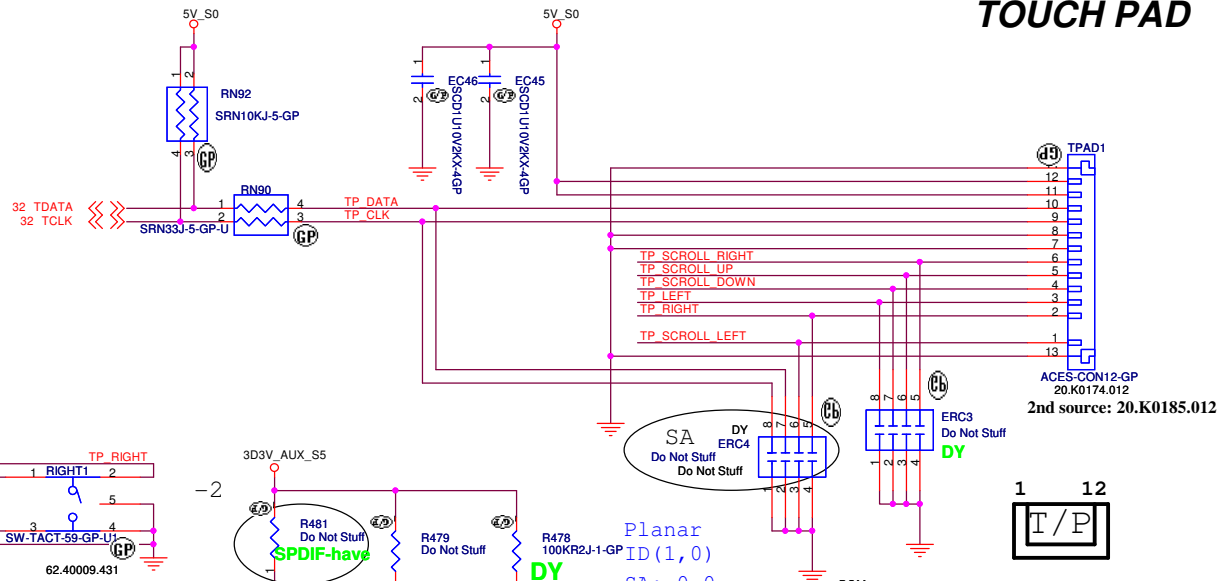


## COVER SWITCH

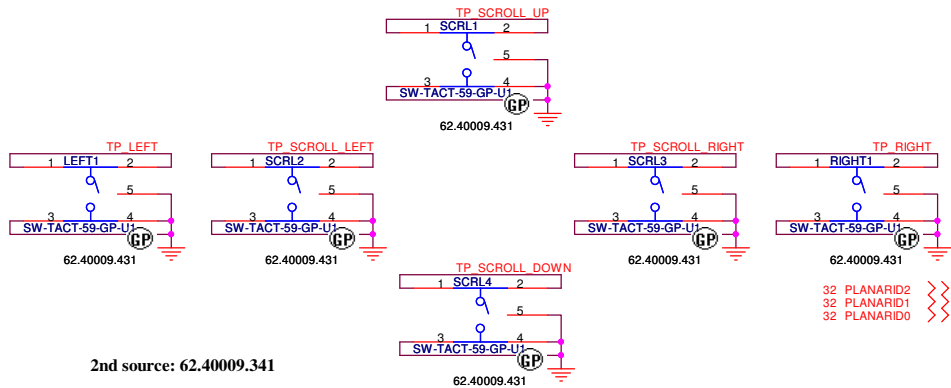


	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

## TOUCH PAD




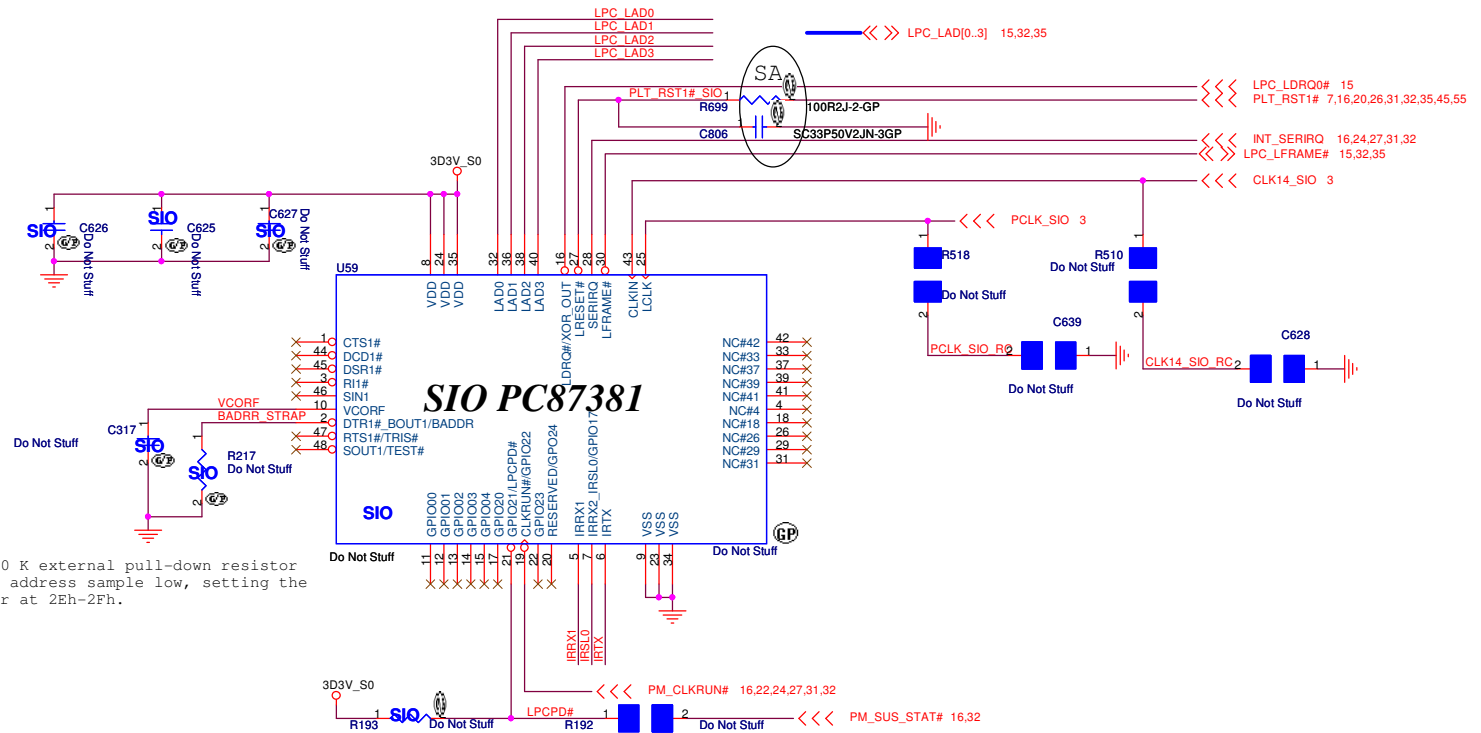
## SCROLL KEY



**2nd source: 62.40009.341**

```
Planar
-GP ID(1,0)
SA: 0,0
01: 0,1
02: 1,0
03: 1,1
```

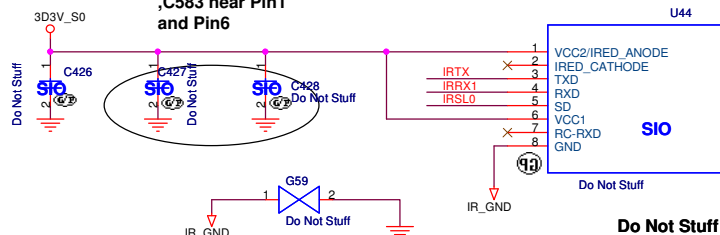
BOM			
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>KEYBOARD/TOUCHPAD</b>			
Size A3	Document Number <b>AG3</b>	Rev <b>2</b>	
Date: Friday, April 21, 2006	Sheet	33 of	55



## VISHAY FIR/CIR Module

Place C581  
,C583 near Pin1  
and Pin6

Layout Guide:  
(1) FIR\_3D3V : 30 mils,  
(2) C583, C581 close  
to U32

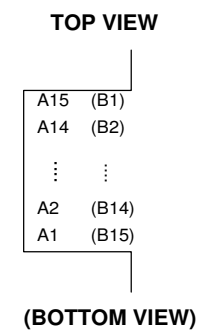
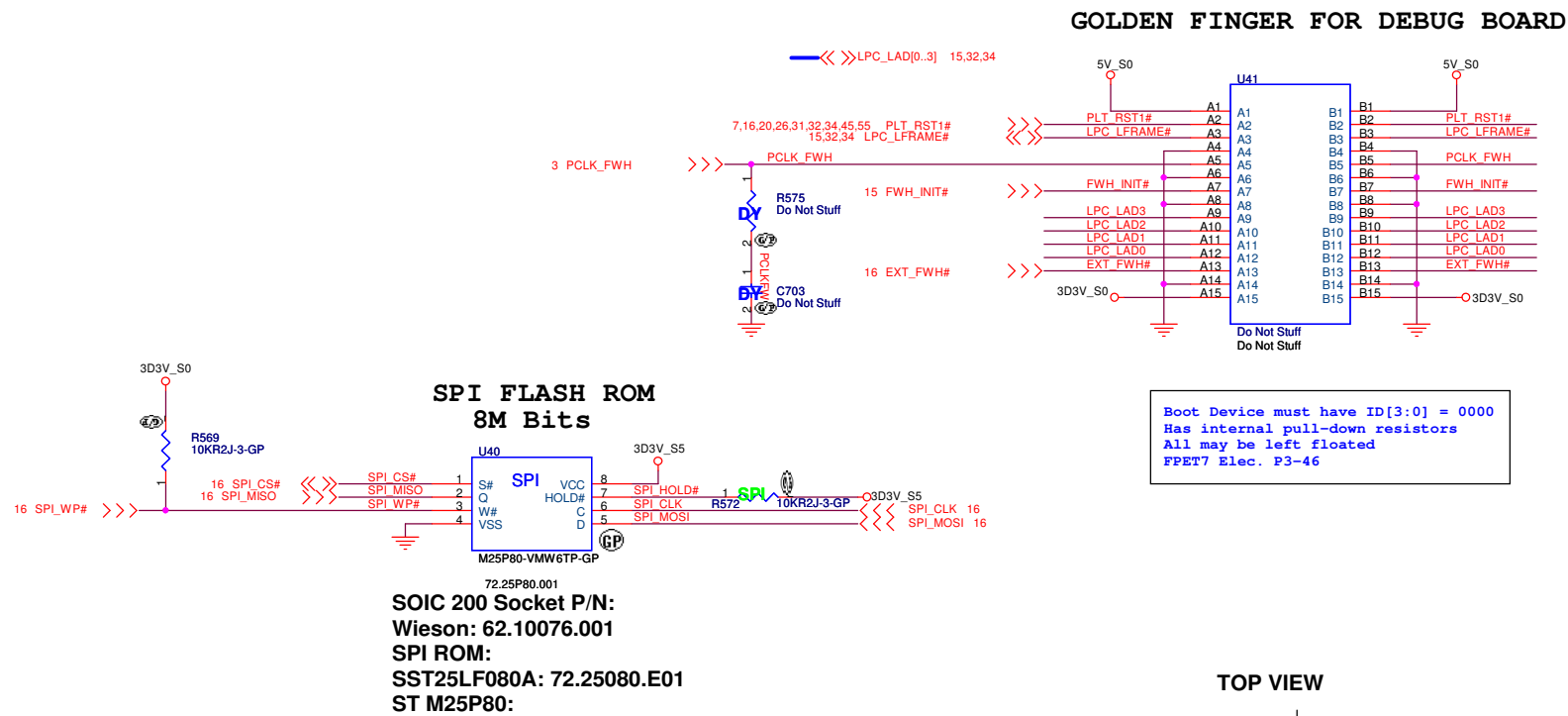


BOM

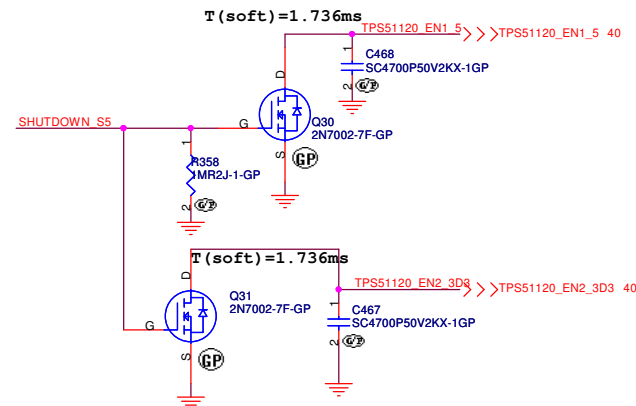
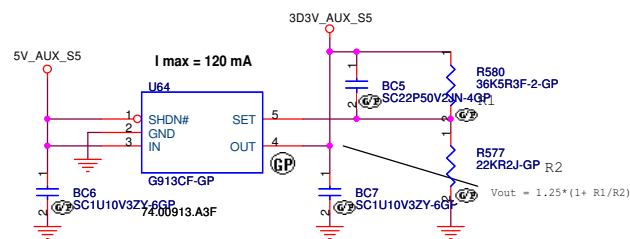
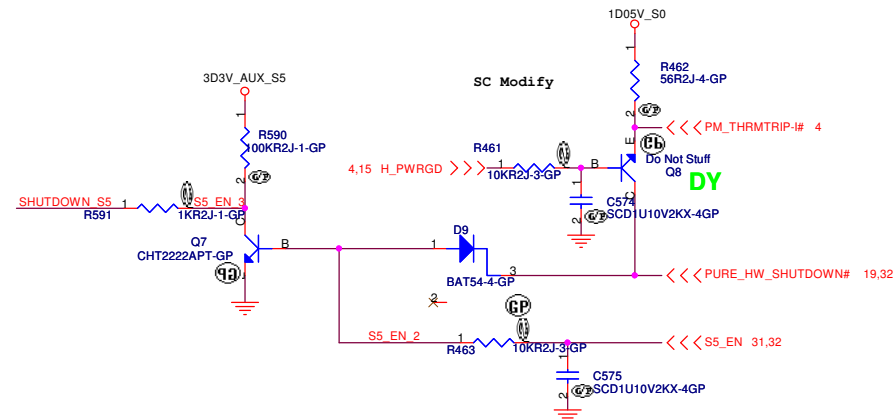
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsein 221, Taiwan, R.O.C.

Title			SIO 87381 / FIR	
Size	Document Number			Rev
A3	AG3			2
Date:	Thursday, April 20, 2006	Sheet	34	of 55

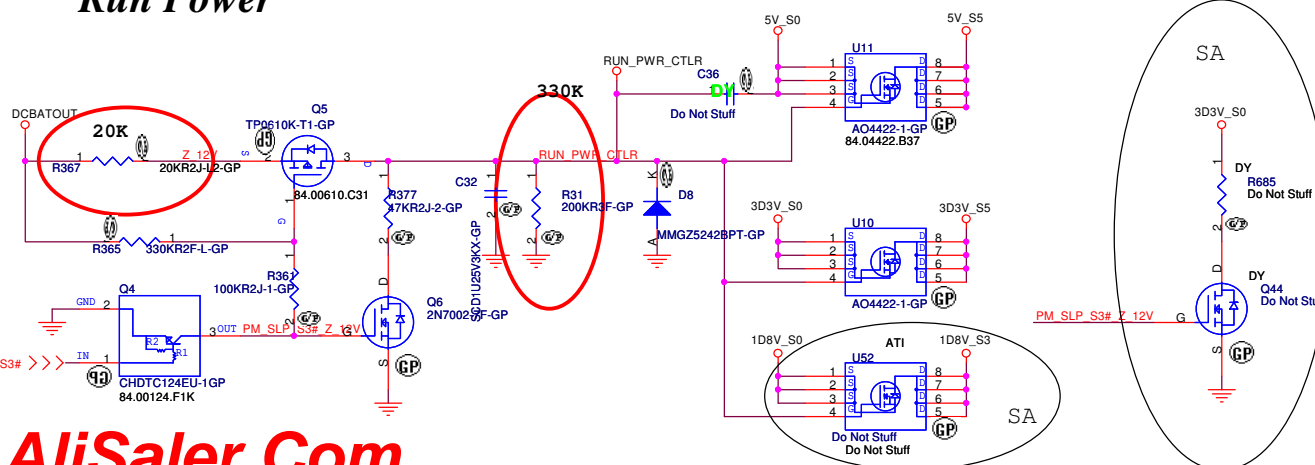




```
*Layout*
15 mil
```



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**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b><i>RUN and AUX POWER</i></b>			
Size A3	Document Number		Rev
	<b>AG3</b>		<b>2</b>
Date:	Thursday, April 20, 2006	Sheet 36 of	55

CPU\_CORE  
Intersil ISL6262

VID Setting		Output Signal
H_VID0	VID0 (I / 1.05V)	PGOOD (OD / 3.3V)
H_VID1	VID1 (I / 1.05V)	
H_VID2	VID2 (I / 1.05V)	
H_VID3	VID3 (I / 1.05V)	
H_VID4	VID4 (I / 1.05V)	
H_VID5	VID5 (I / 1.05V)	
H_VID6	VID6 (I / 1.05V)	
Input Signal		Output Power
PSI#	PSI# (I / 3.3V)	
CPUCORE_ON	PGD_IN (I / 3.3V)	
PM DPRSLPVR	DPRSLPVR (I / 3.3V)	
H DPRSTP#	DPRSTP# (I / 3.3V)	
Voltage Sense		Output Power
VCC_SENSE	VSEN (I / Vcore)	
VSS_SENSE	RTN (I / Vcore)	
Input Power		Output Power
DCBATOUT_6262	VCC (I)	
5V_S0	VCC (I)	
3D3V_S0	VCC (I)	

6262\_PWRGOOD

CLK\_EN# (O)

VCC\_CORE\_S0 (Imax=48A)

TI TPS51116  
1.8V / 0.9V

Input Signal		Output Signal
PM_SLP_S5#	S5	PGOOD (OD / 3.3V)
	S3	
Input Power		Output Power
DCBATOUT	VCC (I)	VCC (O)
5V_S5	VCC (I)	VCC (O)

CPUCORE\_ON

1.8V\_S3

0.9V\_S0

ISL6269\_1D2V

Input Signal		Output Power
1D2V_S0_EN	SS_STBY1 (I / 5V) FOR 1.2V	1D2V_PWR
DCBATOUT_6269	VIN	

2D5V\_S0

3D3V_S0	INPUT	OUT	2D5V_S0
---------	-------	-----	---------

APL5332KAC

1D5V\_S0

1D8V_S3	INPUT	OUT	1D5V_S0
---------	-------	-----	---------

APL5912-KAC-GP

1D05V\_S0

1D8V_S3	INPUT	OUT	1D05V_S0
---------	-------	-----	----------

APL5912-KAC-GP\* 2

1D2V\_S0

1D8V_S0	INPUT	OUT	1D2V_S0
---------	-------	-----	---------

APL5331KAC-TRL

TPS51120  
5V/3D3V

Input Signal		Output Signal
TPS51120_EN1_5	EN1	PGOOD1 (OD / 5V)
TPS51120_EN2_3D3	EN2	PGOOD2 (OD / 5V)
Input Power		Output Power
DCBATOUT_TPS51120	VIN	5V (O)
		3D3V (O)

CPUCORE\_ON

CPUCORE\_ON

5V\_DC\_S5 (6A)

3D3V\_DC\_S5 (5A)

CHARGER ISL6225

Input Signal		Output Signal
CHGON#/OFF	ICTL	BATT
BT_TH	PKPRES	ACOK
Input Power		Output Power
AD+	ACIN	VOUT (O)
		VOUT (O)

BT+SENSE

AC\_IN

BT+

DCBATOUT

3D3V\_AUX\_S5

5V_S5_G913	INPUT	OUT	3D3V_AUX_S5
------------	-------	-----	-------------

G913CF

5V\_AUX\_S5

DCBATOUT	INPUT	OUT	5V_AUX_2591
----------	-------	-----	-------------

LP2951ACM

Adapter

Input Signal		Output Signal
AD_OFF	(I)	(O)
AD_JK	VCC (I)	VCC (O)
5V_AUX_S5	VCC (I)	VCC (O)

AD\_IN

AD+

BOM

<b>緯創資通</b> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	<b>Power Block Diagram</b>
Size A3	Document Number <b>AG3</b>
Date: Thursday, April 20, 2006	Rev <b>2</b>
Sheet 37	of 55

Place close to phase 1 choke  
If NTC=330Kohm, R10=8.66K

When test without cpu,  
R183 & R184 change to 0 ohms  
If VCC\_SENSE and VSS\_SENSE pins have pulled  
resistors to VCC\_CORE\_S0  
==> Remove R183/R184

PGOOD  
Power good open-drain output.  
Will be pulled up externally by  
a 680. resistor to VCCP or 1.9k. to 3.3V.

OCP>=50A

Load Line

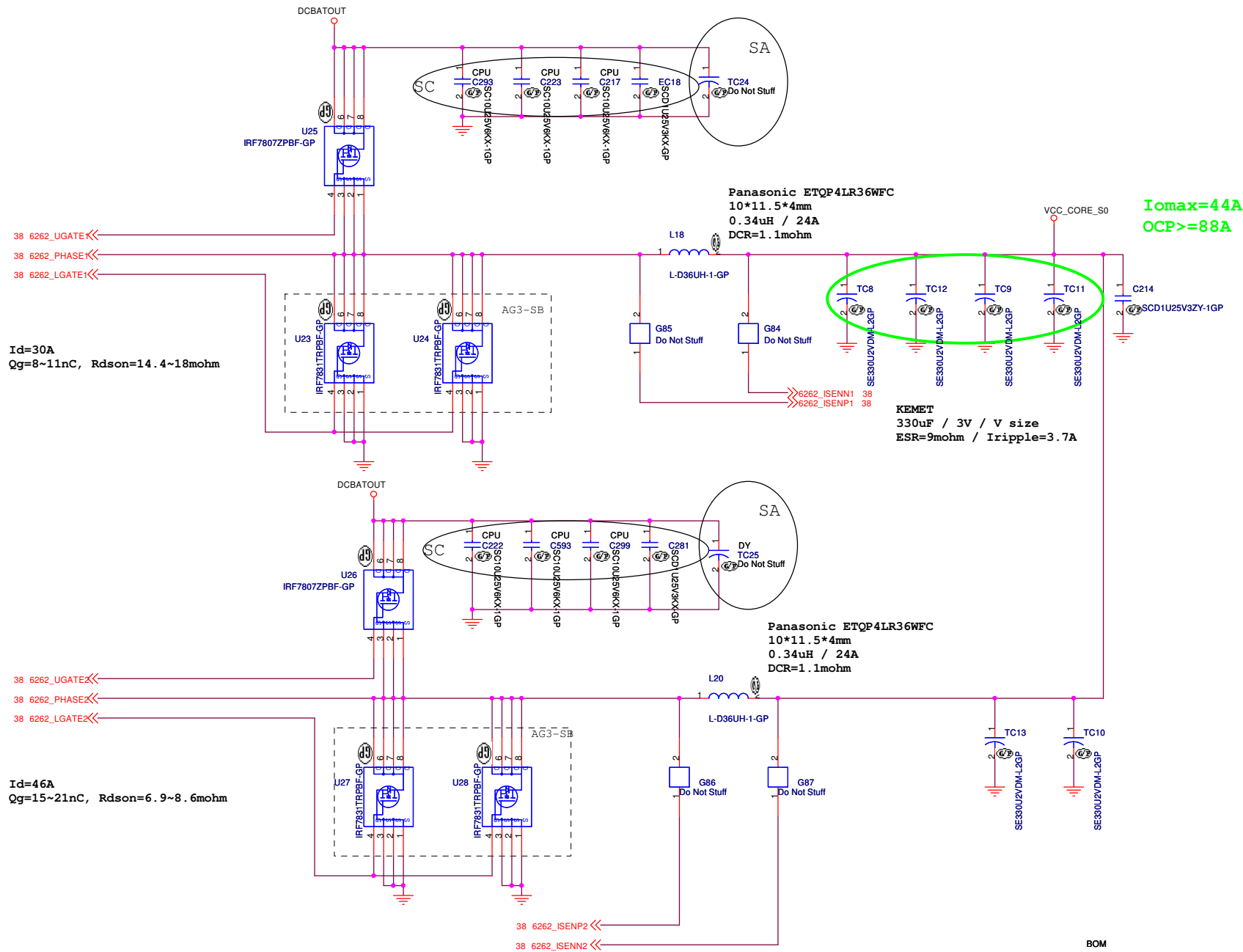
Place close to phase 1 choke

Switching Frequency=300KHz

BOM

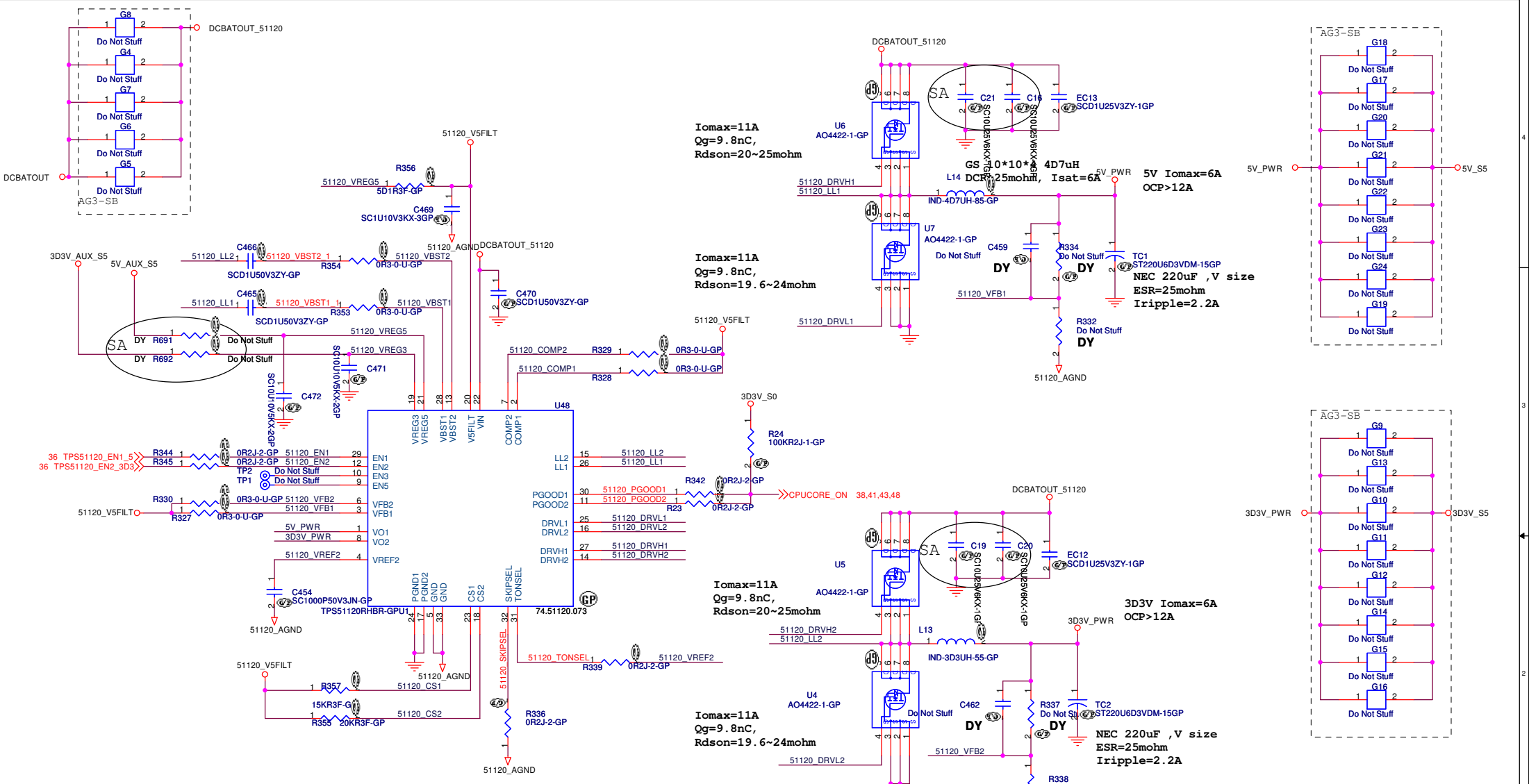
Title		
CPU Vcore Power_1		
Size A3	Document Number	Rev 2
AG3		
Date: Thursday, April 20, 2006	Sheet 38	of 55

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BOM

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Title <b>CPU Vcore Power_2/2</b>	
Size A3	Document Number <b>AG3</b>
Date: Friday, April 21, 2006	Sheet 39 of 55 Rev <b>2</b>



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switcher ON	Switcher ON

$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,  
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

BOM

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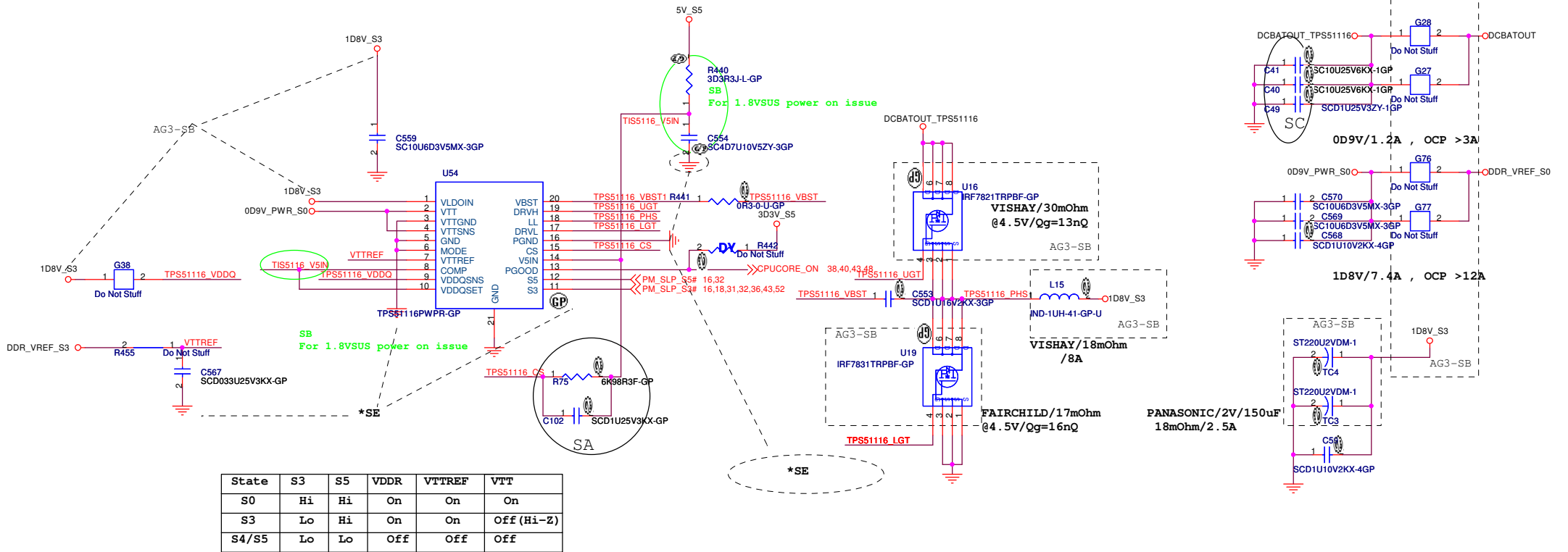
Title: **5V\_UP\_S5/3D3V\_S5/5V\_S5**

Size A3 Document Number **AG3** Rev **2**

Date: Thursday, April 20, 2006 Sheet 40 of 55



# TI TPS51116 for 1D8V and 0D9V

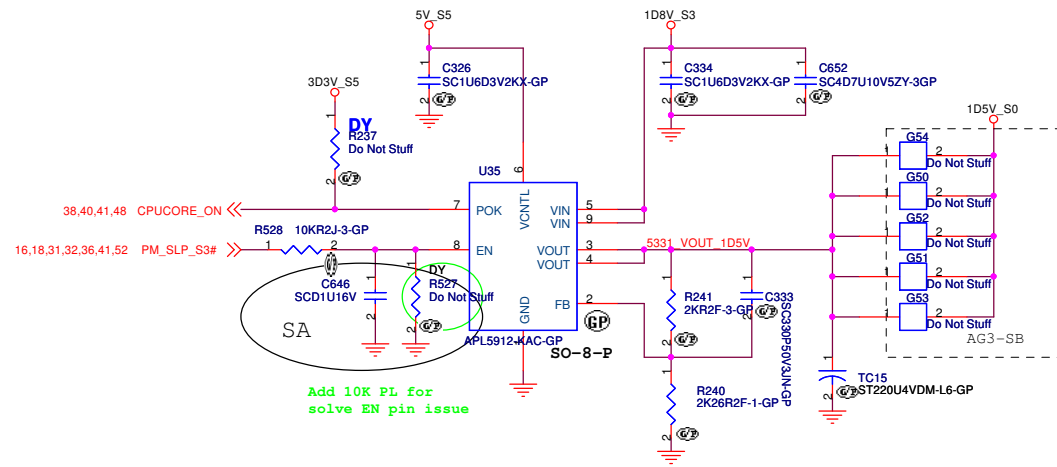
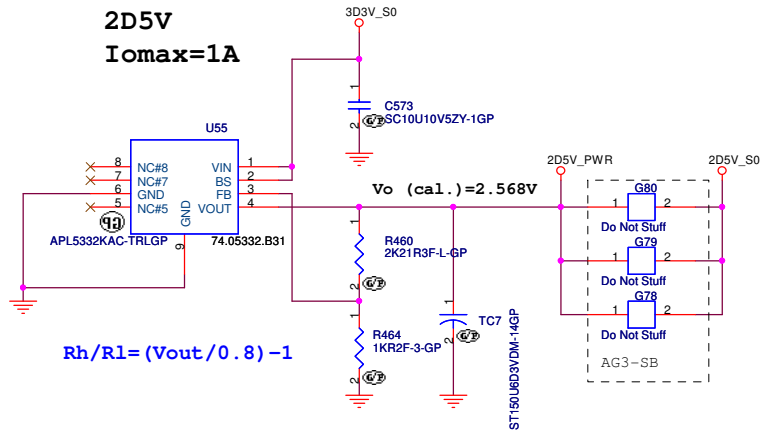


BOM

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>DC to DC 1.8V &amp; 0.9V</b>	
Title Size A3 Date: Friday, April 21, 2006	Document Number <b>AG3</b> Sheet 41 of 55
Rev <b>2</b>	



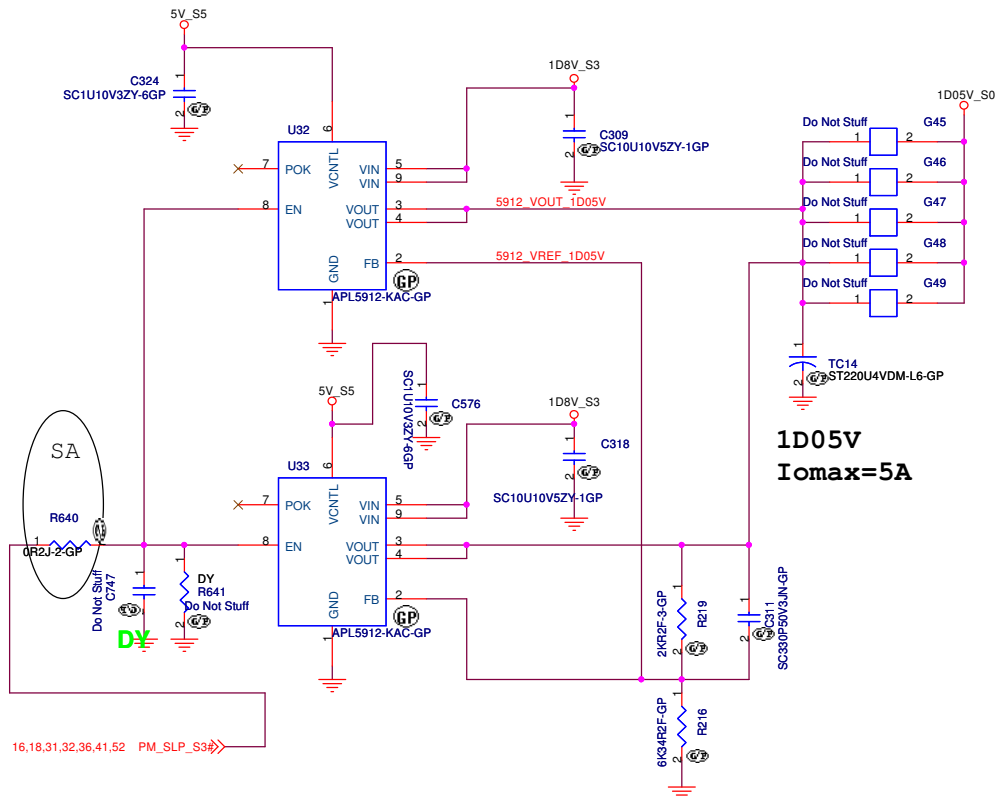
## 2D5V Iomax=1A



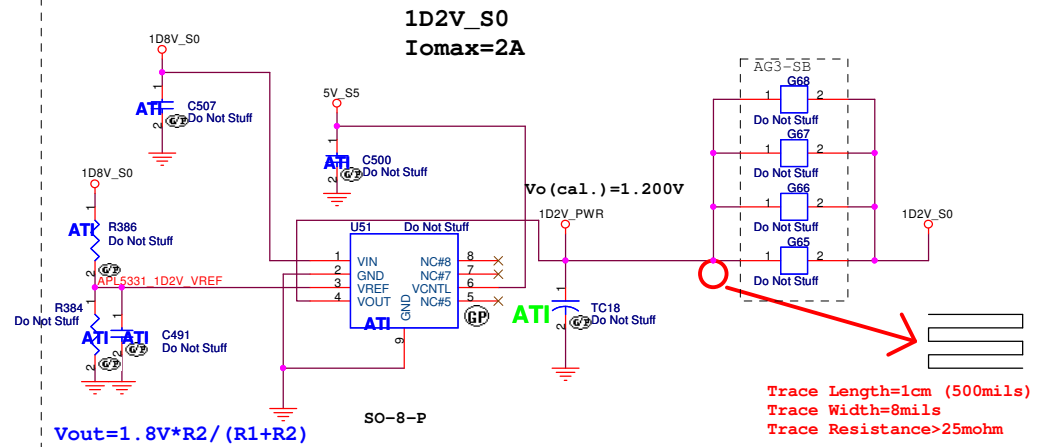
KEMET  
100uF, 6V, B2 Size  
ESR=40mohm

$$V_o = 0.8 * (1 + (R_1/R_2))$$

AG3-SB



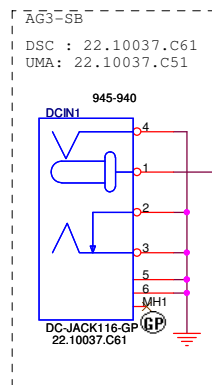
## 1D05V Iomax=5A



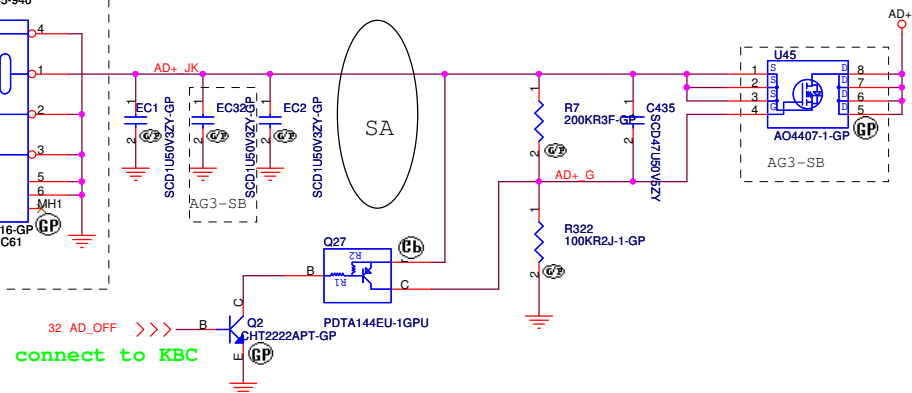
## 1D2V\_S0 Iomax=2A

BOM

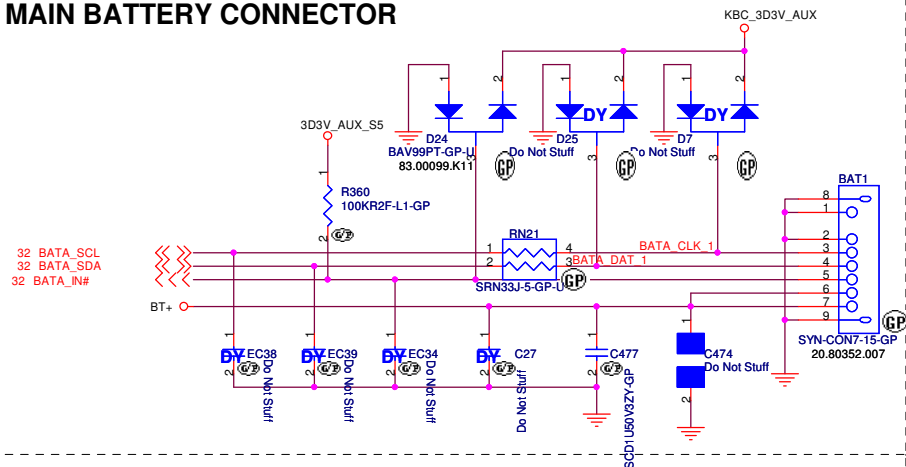
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
1D2V/1D5V/2D5V/1D05V_S0		
Size	Document Number	Rev
A3	AG3	2
Date:	Thursday, April 20, 2006	Sheet 43 of 55



## ADAPTER IN CIRCUIT



## MAIN BATTERY CONNECTOR

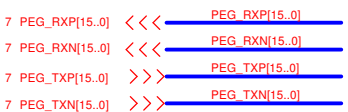


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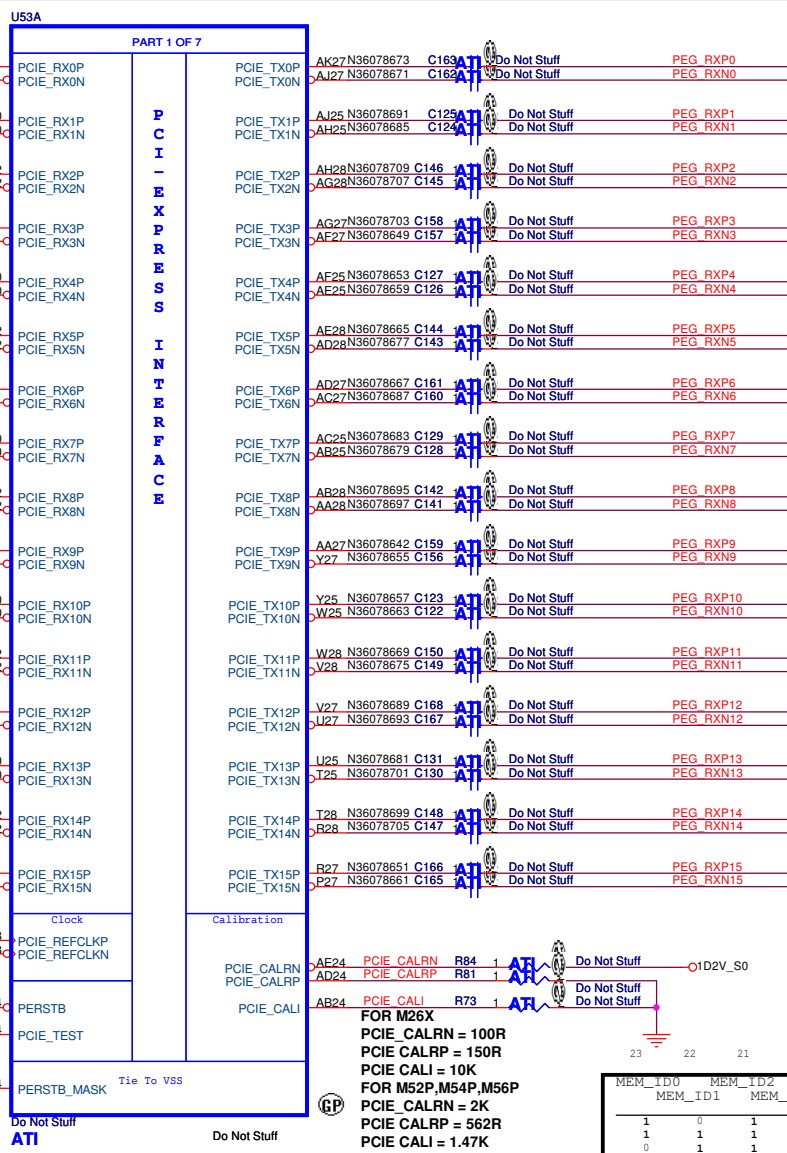
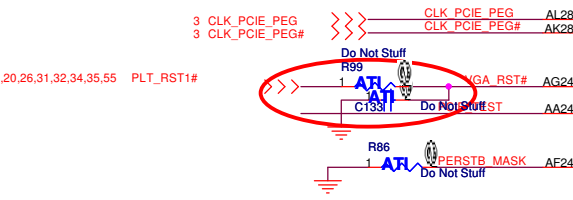
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
AD/BATT CONN		
Size	Document Number	Rev
A3	AG3	2
Date:	Friday, April 21, 2006	Sheet 44 of 55

PCIE TEST PADS  
PCIE TEST POINTS MUST BE WITHIN 250 MILS  
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE  
SIGNALS THE SAME DISTANCE



PCIE SIGNALS CONNECT TO ROOT COMPLEX  
REFER TO PCI EXPRESS DESIGN GUIDE  
FOR RECOMMENDED AC COUPLING CAPS  
PLACEMENT ALONG THE TX INTERCONNECT

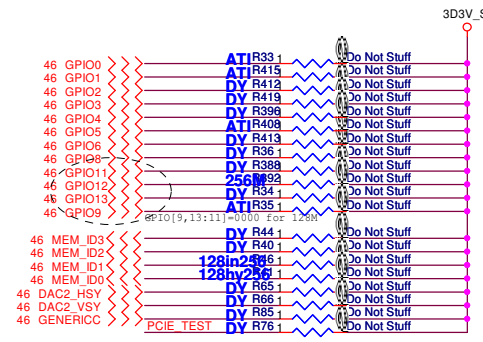


M56: 71.0M56P.M01  
M54: 71.0M54P.B0U  
M52: 71.0M52P.B0U

FOR M26X  
PCIE\_CALRN = 100R  
PCIE\_CALRP = 150R  
PCIE\_CALI = 10K  
FOR M52P,M54P,M56P  
PCIE\_CALRN = 2K  
PCIE\_CALRP = 562R  
PCIE\_CALI = 1.47K

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPS
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Infineon	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0)	GPIO[9,13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM	1011
MEMORY APERTURE SIZE	GPIO[13:11]	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERTURE SETTINGS	TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICCC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	



When no ROM is attached, GPIO[9] is set to 0.  
GPIO[13:12] is used to select the frame buffer aperture size.  
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00  
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01  
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10  
GPIO[13:12] = 11: reserved, same as ROM strap 11

BOM

緯創資通

Wistron Corporation

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Title		
ATI M5X-P PCIE 1/4		
Size	Document Number	Rev
A3	AG3	2
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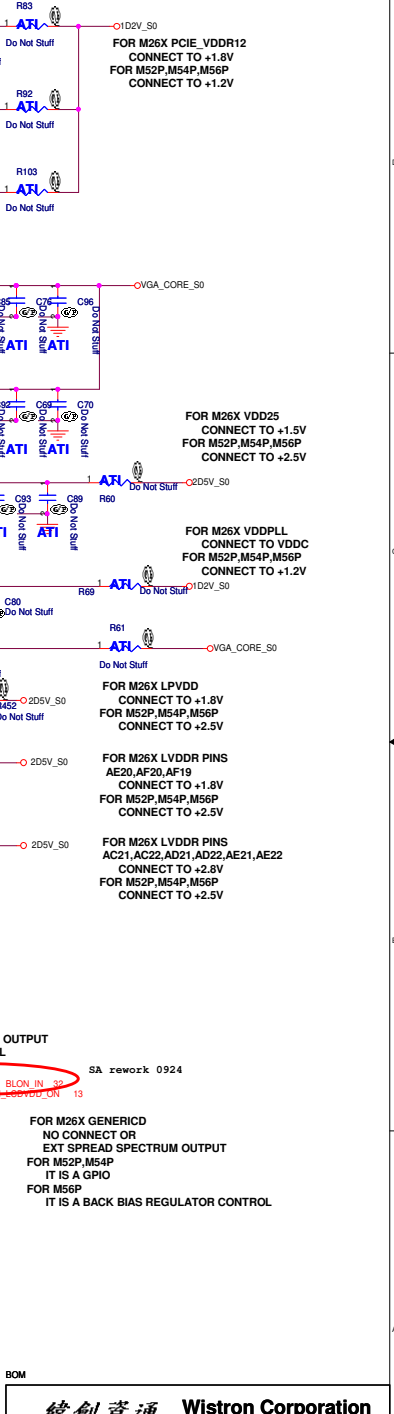
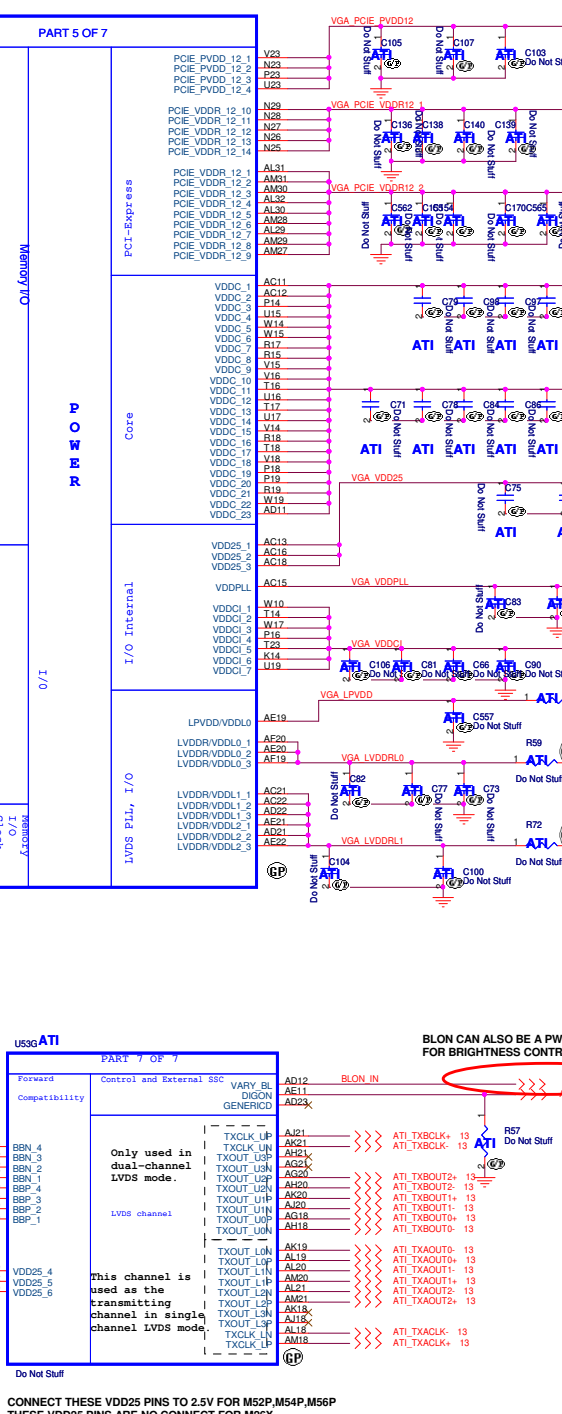
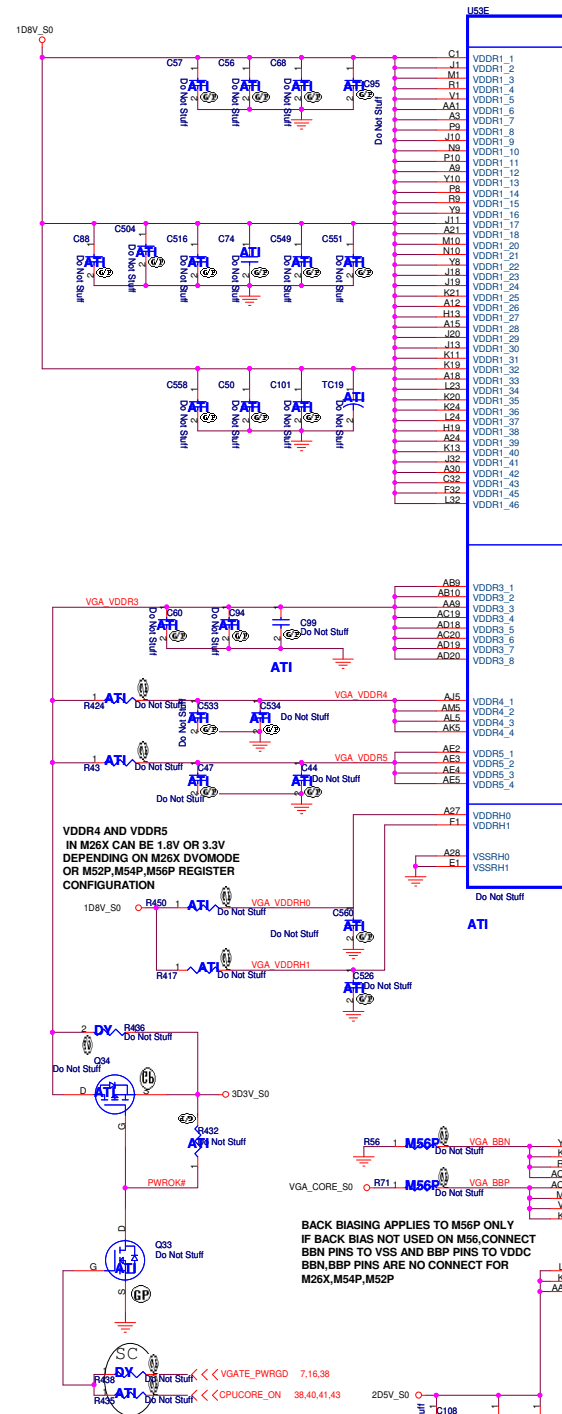
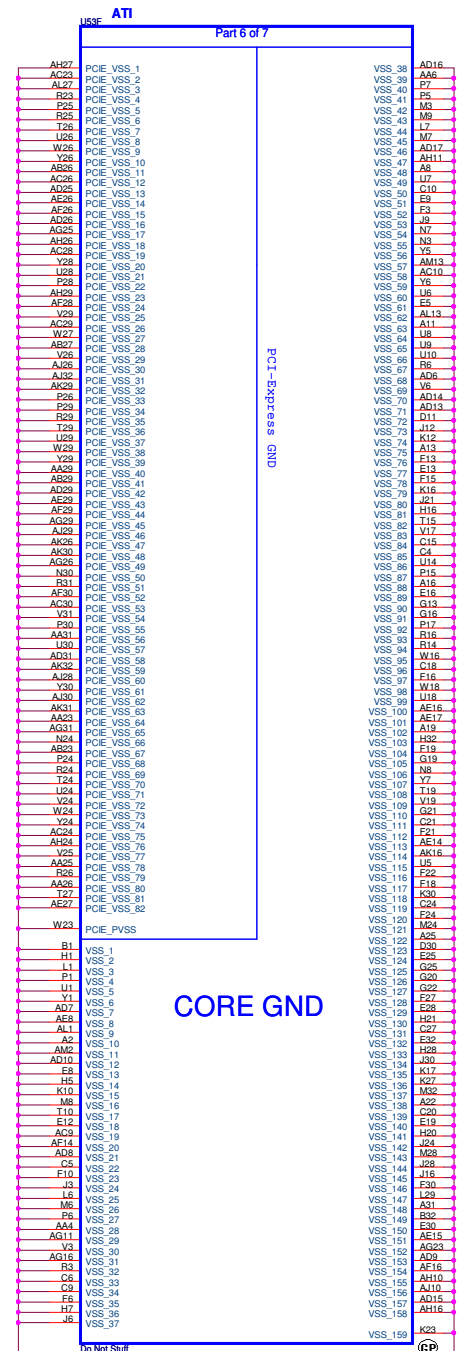


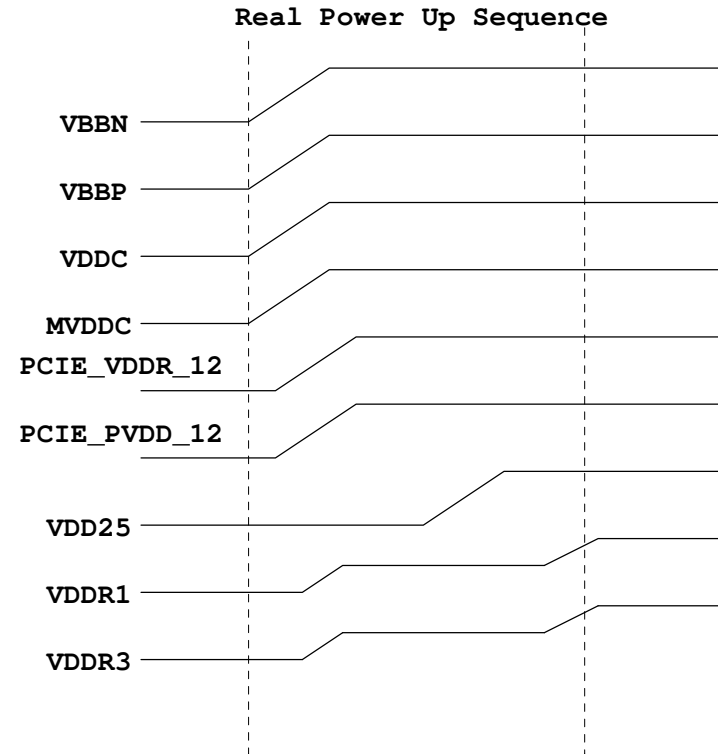
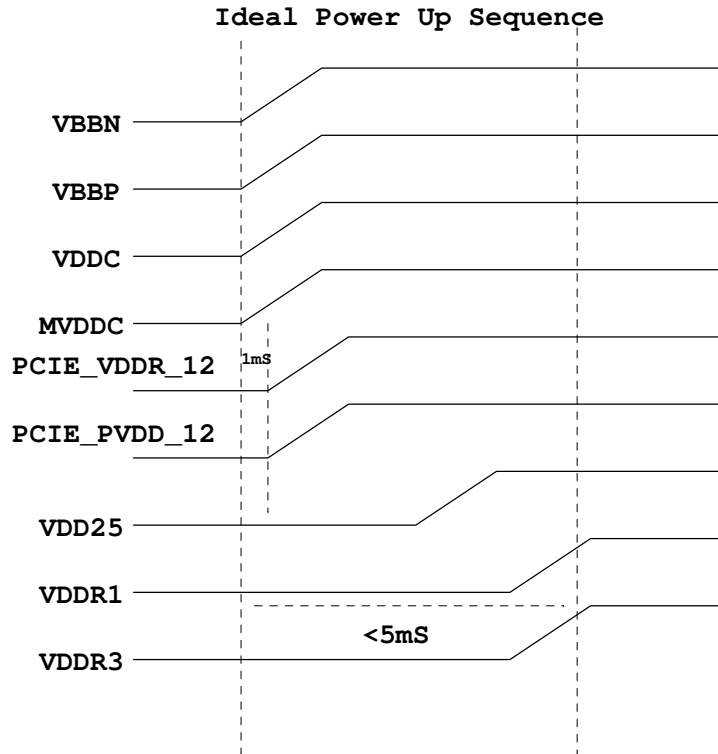
PIN B25 IS MA14 (BA0)  
PIN C25 IS MA15 (BA1)  
PIN E29 IS MA13 (BA2)  
PIN E27 IS MA12



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Title			
<b>ATI M5X-P MEM 3/4</b>			
Size A3	Document Number		Rev
	<b>AG3</b>		<b>2</b>
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance  
For the value, it can be read by the number before R. (R means resistor)  
For the tolerance, it can be read from the last letter.  
For the rating, we don't show on the symbol name.  
For the size, R2=>0402, R3=>0603, R5=>0805,.....

General Guidelines:

- BBN and BBP must ramp up before or at the same time as VDDC but not after.
- VDDC and MVDDC must be ramped up first, followed by PCIE\_VDDR\_12, PCIE\_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).
- All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).
- VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.
- The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory I/Os) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:  
Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

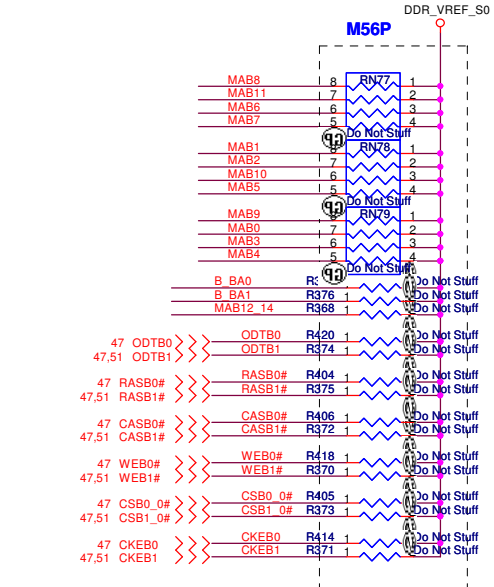
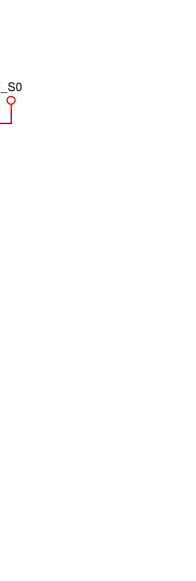
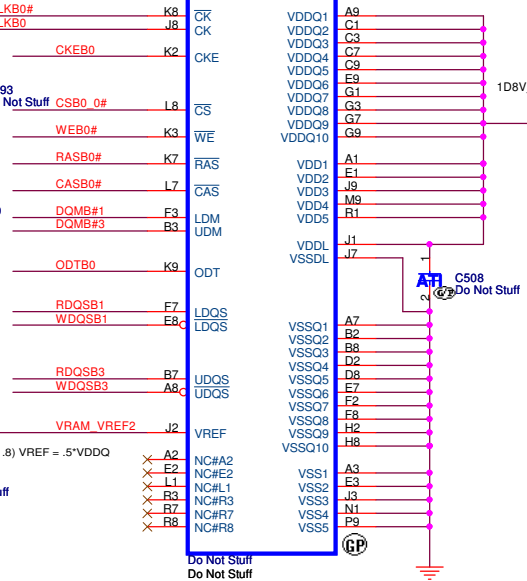
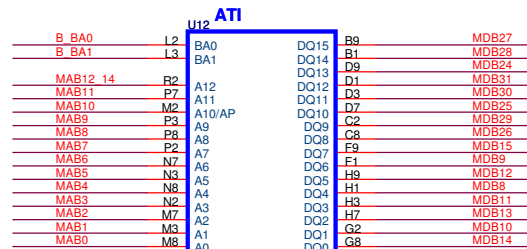
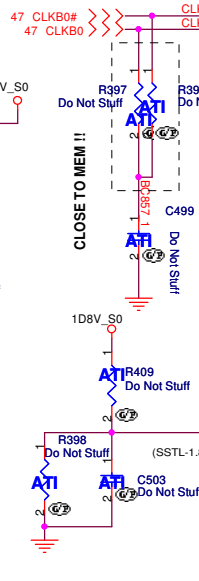
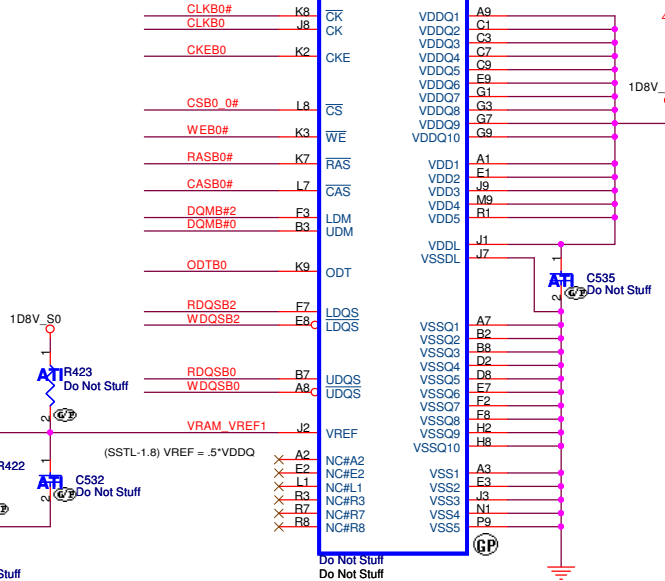
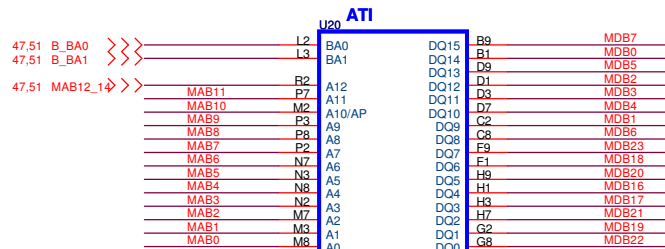
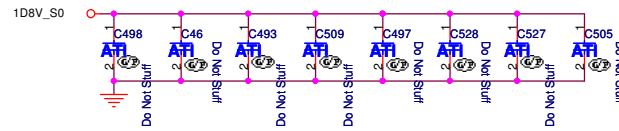
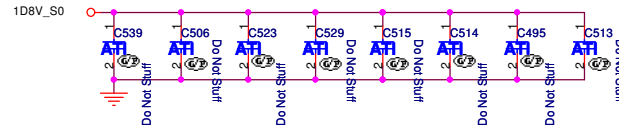
Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating ( X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3 )	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is  
Capacitor type + value + rating + size + tolerance + material  
SCD1U10V2MX-1  
SC=> SMT Ceramic, TC=> POS cap or SP cap  
D1U => 0.1uF  
10V => the voltage rating is 10V  
2=> 0402, 3=>0603, 5=>0805  
M=>tolerance J, K, M, Z  
X=> X7R/X5R, Y=> Y5V  
-1 => symbol version, nonsense to EE characteristic

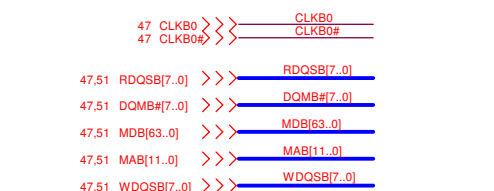
BOM

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Title <b>ATI M5X-P POWER SEQUENCE</b>		
Size A3	Document Number <b>AG3</b>	Rev <b>2</b>
Date: Thursday, April 20, 2006 1 of 55		

# CHAN B DDR2 84BGA 32MX16 MEMORY

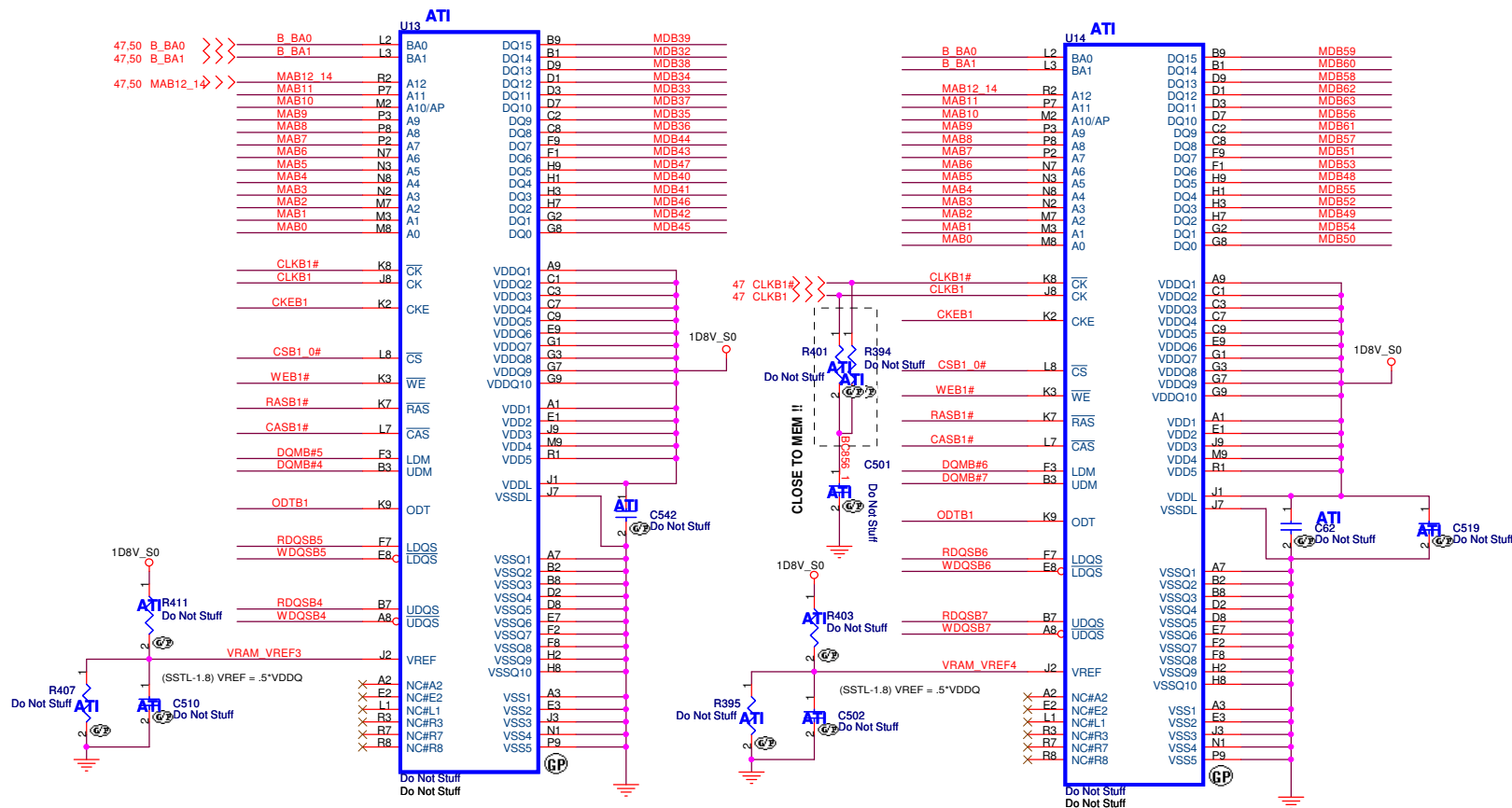
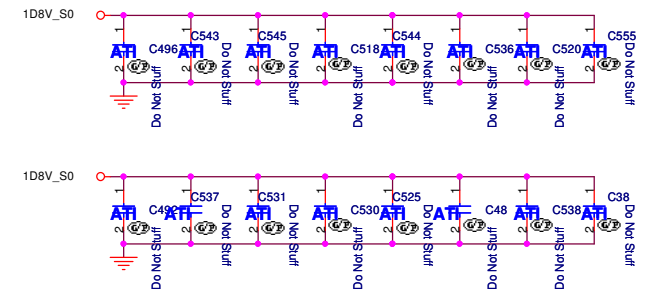


FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ  
MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT  
AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP  
TO A VTT RAIL (50% OF VDDQ)



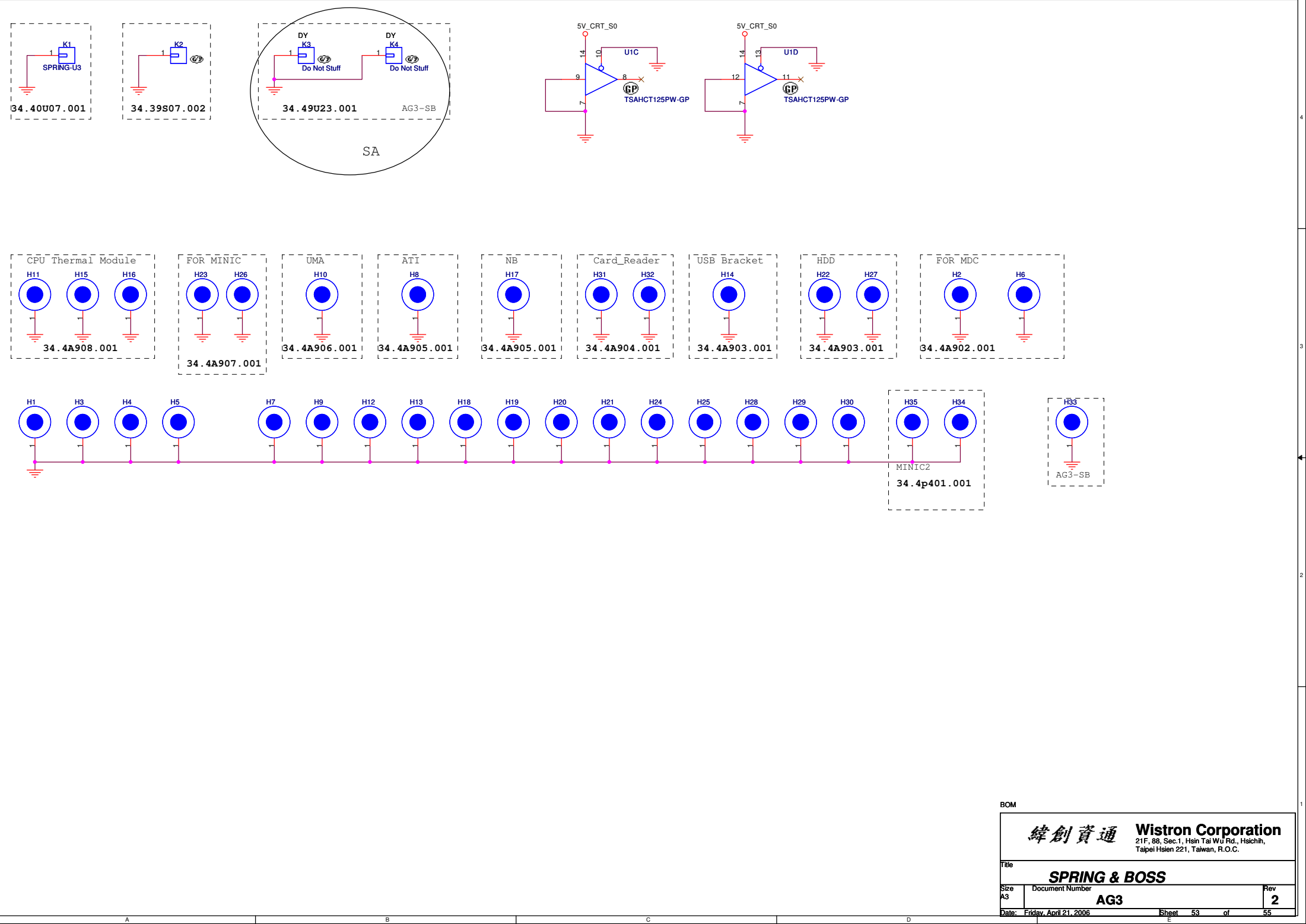
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M\*16, 350Mhz)  
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA (16M\*16, 350Mhz)  
72.18512.A0U IC VRAM HYB18T512161BF-25 BGA (32M\*16, 400Mhz)

BOM	
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File	
<b>VRAM 1/2</b>	
Size	Document Number
A3	AG3
Date: Thursday, April 20, 2006	Sheet 50 of 55





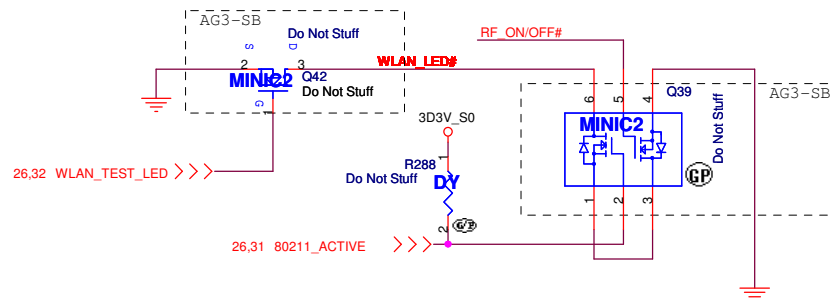
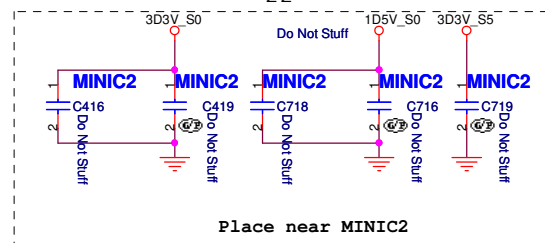
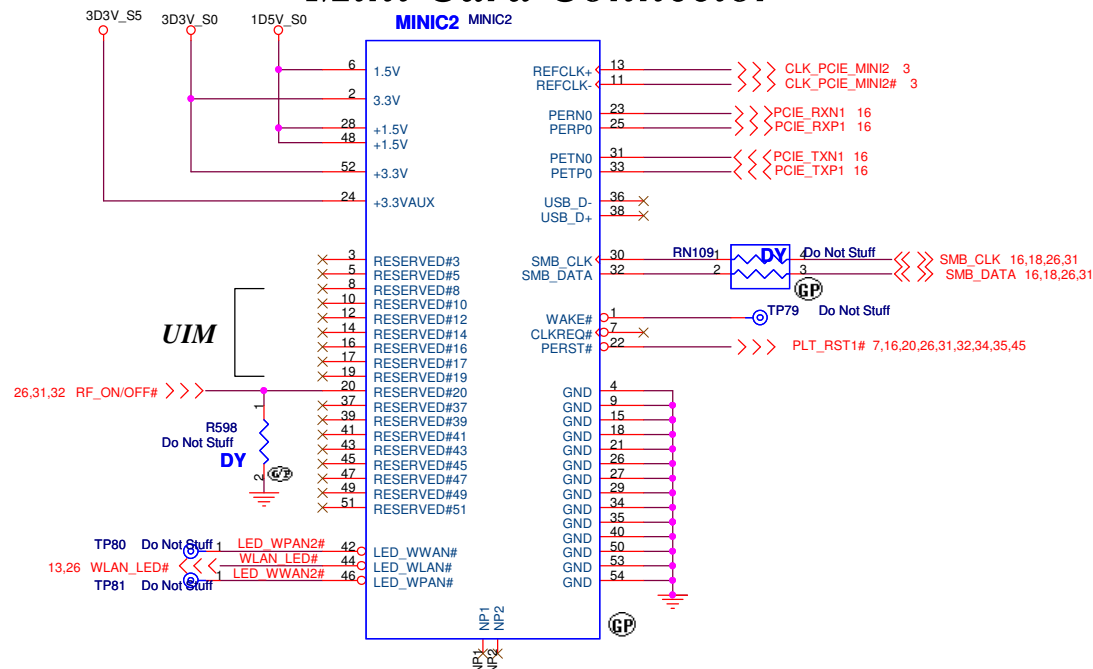




## AG3-SB



# Mini Card Connector



BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>MINICARD 2</b>		
Size	Document Number	Rev
B	<b>AG3</b>	<b>2</b>
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